SHORT BIOGRAPHY

Chun-Lung Hsu received the Ph.D. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C. in 2000. Hsu worked as an assistant/associate professor at the Department of Electrical Engineering, National Dong Hwa University (NDHU), Hualien, Taiwan, R.O.C. from 2000 to 2011. The major research of his laboratory is low-power circuit design, VLSI design/testing and tolerance scheme development for image system. In the Autumn of 2011, Hsu changed the working field from academia to research unit, the Information & Communication Laboratory (ICL) and the Electronic & Optoelectronic System Laboratory (EOSL), Industrial Technology Research Institute (ITRI) that located in HsinChu. For more than 10-year work experiences in Industrial and Academic cooperation projects, Hsu have accumulated a lot of technical knowledge and practical experiences in ultra low-power SoC design, heterogeneous stacking IC design/testing, high-level synthesis design for embedded system, mobile devices testing and artificial intelligence (AI) deep learning technologies. In other words, Hsu have rich experiences in teaching, research, and project planning and executing. Hsu is now working at the Department of Electrical Engineering, National Center University (NCU), Taoyuau, Taiwan, R.O.C. The IICD (Intelligent Integrated Circuit Design) laboratory of Hsu is focused on the research of SW/HW co-design for deep learning accelerator chip design, data-driven energy-efficiency chip design, SDC (software-defined chip/chiplet) EDA technology and GAI (Generative AI) chip design technology, Also, Hsu is now a member of the IEICE, IET, and IEEE Society.

EDUCATION

- Sep. 1996 - June 2000
  Ph.D., Institute of EE, National Taiwan University
- Sep. 1989 - June 1991
  M.S., Institute of EE, National Cheng Kung University
- Sep. 1986 - June 1988
  B.S., Dept. EE, National Taiwan University of Science and Technology

Work Experience

- Feb. 2024 ~
  Dept., EE, Associate Professor, National Central University
- Aug. 2011 – Jan. 2024
  Principal Engineer and Director, ICL & EOSL, ITRI
- Aug. 2016 – Jan. 2017
  Dept., EE, Adjunct Associate Professor, National Taiwan University of Science and Technology
- Feb. 2016 - July 2016
  Dept., EE, Adjunct Associate Professor, National Chiao Tung University
- Aug. 2006 - July 2011
  Dept., EE, Associate Professor, National Dong Hwa University
- Aug. 2001 - July 2006
  Dept., EE, Assistant Professor, National Dong Hwa University
- Aug. 2000 - July 2001
  Dept., EE, Associate Professor, LungHwa University of Science and Technology
- Aug. 1991 - July 2000
  Dept., EE, Lecturer, LungHwa University of Science and Technology
- Aug. 1988 - July 1989
  Dept., EE, Teaching Assistant, MingChi University of Technology

Research Interests

- SW/HW co-design for deep learning accelerator chip design
- Data-driven energy-efficiency chip design
- SDC (software-defined chip/chiplet) EDA technology
- GAI (Generative AI) chip design technology