



Journal Papers

1. K. S. Li, X. J. Leon, L. Y. Chen, S. J. Wang, Y. A. Huang, J. E. Chen, H. C. Liang, and *C. L. Hsu, "Wafer Defect Pattern Labeling and Recognition Using Semi-supervised Learning," *IEEE Transaction on Semiconductor Manufacturing (TSM)*, vol. 35, issue. 2, pp. 291-299, May. 2022. (SCI).
2. K. S. Li, L. Y. Chen, Y. Y. Liao, S. J. Wang, Y. A. Huang, L. Chou, C. Y. Tsai, C. C. Cheng, C. H. Han, C. S. Lee, J. E. Chen, H. C. Liang, and *C. L. Hsu, "Wafer Scratch Pattern Reconstruction for High Diagnosis Accuracy and Yield Optimization," *IEEE Transaction on Semiconductor Manufacturing (TSM)*, vol. 35, issue. 2, pp. 272-281, May. 2022. (SCI).
3. S. K. Lu, H. P. Li, K. Miyase, *C. L. Hsu, and C. T. Sun, "Fault-Aware Dependability Enhancement Techniques for Phase Change Memory," *J. Electronic Testing: Theory and Applications (JETTA)*, vol. 37, no. 4, pp. 503-513, Aug. 2021. (SCI)
4. K. C.-C. Cheng, L. L.-Y. Chen, J.-W. Li, K. S.-M. Li, N.C.-Y. Tsai, S.-J. Wang, A.Y.-A. Huang, L. Chou, C.-S. Lee, J.E. Chen, H.-C. Liang, and *C.-L. Hsu, "Machine Learning Based Detection Method for Wafer Test Induced Defects," *IEEE Transactions on Semiconductor Manufacturing (TSM)*, vol. 34, issue. 2, pp. 161-167, May. 2021. (SCI)
5. K. S.-M. Li, P.Y.-Y. Liao, K.C.-C. Cheng, L.L.-Y. Chen, S.-J. Wang, A.Y.-A. Huang, L. Chou, G.C.-H. Han, J.E. Chen, H.-C. Liang, and *C.-L. Hsu, "Hidden Wafer Scratch Defects Projection for Diagnosis and Quality Enhancement," *IEEE Transactions on Semiconductor Manufacturing (TSM)*, vol. 34, issue. 1, pp. 9-16, Feb. 2021. (SCI)
6. T. Sugiarto, *C. -L. Hsu, C. -T. Sun, W. -C. Hsu, S. -H. Ye and K. -T. Lu, "Surface EMG vs. High-Density EMG: Tradeoff Between Performance and Usability for Head Orientation Prediction in VR Application," in *IEEE ACCESS*, vol. 9, pp. 45418-45427, 2021.
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8. S. K. Lu, H. K. Huang, *C. L. Hsu, C. T. Sun, and K. Miyase, "Retention-Aware Refresh Techniques for Reducing Power and Mitigation of Data Retention Faults in DRAM," *J. Electronic Testing: Theory and Applications (JETTA)*, vol. 35, no. 4, pp 485-495, Aug. 2019. (SCI)

9. Kun-Lun Luo, Ming-Hsueh Wu, *Chun-Lung Hsu and Chen-An Chen, "Built-in Self-Test Design for the 3D-Stacked Wide-I/O DRAM", *Journal of Electronic Testing: Theory and Applications*, vol. 32, number 2, pp. 111-123, Feb., 2016 (SCI).
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1. S. K. Lu, W. C. Tsai, *C. L. Hsu, C. T. Sun, and Y. A. Yang, "Scrubbing-Based Reliability and Yield Enhancement Techniques for Flash Memories," in *Proc. VLSI Test Technology Workshop (VTTW)*, July 2021.
2. S. K. Lu, Z. L. Tsai, *C. L. Hsu and C. T. Sun, "Fault-Aware ECC Techniques for Reliability Enhancement of Flash Memory," *International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, pp. 1-2, Aug. 2020.
3. S. K. Lu, Z. L. Tsai, *C. L. Hsu, and C. T. Sun, "ECC Caching Techniques for Protecting NAND Flash Memories," in *Proc. IEEE Int'l Test Conf. in Asia (ITC-Asia)*, pp. 47-52, Sep. 2020.
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5. T. Sugiarto, *C. -L. Hsu, C. -T. Sun, S. -H. Ye, K. -T. Lu and W. -C. Hsu, "Head-Orientation-Prediction Based on Deep Learning on sEMG for Low-Latency Virtual Reality Application," [2020 FOURTH IEEE INTERNATIONAL CONFERENCE ON ROBOTIC COMPUTING \(IRC\), 2020](#).
6. S. -R. Lin, W. -H. Lin, S. -H. Huang, *C. -L. Hsu and C. Sun, "Low-Power Hardware Architecture for Depthwise Separable Convolution Unit Design," [2020 IEEE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS - TAIWAN \(ICCE-TAIWAN\), 2020](#).
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15. Chang-Hsin Cheng, *Chun-Lung Hsu, Chung-Kai Liu and Shih-Yin Lin, "High Reliability Built-in Self-Detection and Self-Correction Design for DCT/IDCT Application", *in Proc. The 24th IEEE Intl. SoC Conference*, pp. 213-218, Dec., Sept., 2011.
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Book Chapter

Yu-Sheng Huang, Chen-Kai Chen, and *Chun-Lung Hsu, "Efficient Built-in Self-Test for Video Coding Cores: A Case Study on Motion Estimation Computing Array", The book "VLSI", ISBN 978-3-902613-50-9, 2009.