IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.Doi Number

Neat Temporal Performance of InGaAs/InAlAs Single Photon Avalanche Diode with Stepwise Electric Field in Multiplication Layers

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"This work was supported in part by the Ministry of Science and Technology in Taiwan (MOST) under grant number 106-2221-E-008 -094 -MY3, 107-2627-E-008-001, 106-2221-E-008 -063 -MY3, 108-2622-E-008-011-CC2, 109-3116-F-008-007)."

ABSTRACT We have incorporated a novel design of stepwise electric field in the multiplication layers to the InGaAs/InAlAs single photon avalanche diodes (SPADs). The stepwise electric field profile aims to circumvent the dilemma between dark count rate, afterpulsing and temporal performance. SPADs with large (240 μm) and small (25 μm) active area are fabricated and characterized. The intrinsic temporal response for large and small SPADs has a full-width at half maximum of 72 and 67 ps respectively. Importantly, the diffusion tail exhibits only about 200 ps full-width at one-thousandth maximum, showing fast and neat temporal characteristics. Such devices also present reasonable dark count rate of 5×10^6 Hz and 3×10^7 Hz and moderate single photon detection efficiency of 32 % and 27 % at about 200 K respectively for large and small devices, manifesting that the avalanche build-up time can be improved without losing the detection performance using our specific design and optimized electric field distribution. Such improvement in temporal performance of SPADs should facilitate their capability in the applications of time-correlated single photon counting and light detection and ranging.

INDEX TERMS Single photon avalanche diode (SPAD), timing jitter, light detection and ranging

I. INTRODUCTION

The technology of single photon detection in the near-infrared wavelength range between 1.0 and 1.7 μm is rapidly growing because of the strong demand in various scientific and industrial fields such as quantum cryptography [1], eye-safe laser detection and ranging (LIDAR) [2], VLSI circuit characterization [3] and optical time domain reflectometry [4]. Single-photon avalanche diodes (SPADs), among other types of single photon detectors (SPDs), are small, cost effective, rugged, easy to integrate into array, revealing its potential and capability in the time-dependent faint light detection.

Over the past decade, considerable research activities put focus on InAlAs based APDs since it is known to provide superior performance using InAlAs as multiplication layer than InP [5]. The thickness of multiplication layer should be carefully chosen so as to increase the gain-bandwidth product without compromising the signal to noise ratio. Unfortunately, the gain-dependent excess noise impedes the maximum gain that can be achieved in APDs. Single photon avalanche diode (SPAD), operating at higher voltage above breakdown in the Geiger-mode, could avoid the issue of the excess noise and offer an alternative of more sensitive receiver.

InAlAs based SPADs have been reported as they are expected to improve performance in terms of breakdown and temperature characteristics [6–10]. The higher avalanche breakdown probability in InAlAs results potentially higher single photon detection efficiency (SPDE). In addition, the avalanche breakdown voltage is less sensitive to the temperature, which offers greater tolerance in adjusting the optimum operation temperature and less stringent power supply circuit design. However, for various reported InAlAs-based SPADs, the dark count rates (DCRs) are several orders higher compared with the InP-based SPADs, which is attributed to the low crystal quality of the InAlAs layer as

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well as the tunneling current from the InAlAs multiplication layer. The DCR can be effectively suppressed only if the issues of crystal quality and tunneling are resolved. Since the tunneling current is caused by high field above the breakdown, the thickness of multiplication layer should be thick enough to avoid reaching the tunneling threshold. However, there are accompanying issues with increasing the thickness of multiplication layer. Firstly, the temporal performance gets worse due to increased spread of the avalanche build-up time. Secondly, the afterpulsing effect becomes serious because it is related to the numbers of defect inside the multiplication layer, which depends linearly on the thickness of multiplication region for a given trap concentration. Consequently, there is a tradeoff between primary DCR, maximum count rate (restricted by the afterpulsing effect) and the temporal performance.

The temporal response of SPADs is an important figure of merit for the applications of time of flight (TOF), time-correlated single photon counting (TCSPC), quantum key distribution (QKD), and so on. It usually consists of a main peak and an exponential tail, where the full width at half maximum is referred to “timing jitter”. For the TOF applications using a SPAD detector, the precision of a distance measurement relies on the timing jitter of the SPAD detector. Although the precision can be improved by accumulating and averaging several TOF measurements, the long exponential tail will widen the standard deviation of the time interval histogram. The exponential tail also limits the bit error rates in quantum key distribution [11] and timing resolution of optical waveform in time-resolved optical spectrometer [12]. Therefore, it is necessary to delicately design SPAD structure not only for a minimal jitter but also for a minimal full-width at one-thousandth maximum.

This work proposes a unique design of stepwise electric field profile in the multiplication layer of InGaAs/InAlAs SPADs [13] and examines such design by characterizing the temporal as well as the detection performance for two different diameter sizes of SPADs (240 μm and 25 μm). The 240 μm and 25 μm SPADs exhibit fast timing jitter of 72 ps and 67 ps and a moderate single photon detection efficiency (SPDE) of 32 % and 27 % under 1.31 μm. The full width at one-thousandth of the maximum for both large and small devices are superior to the reported InGaAs/InP and InGaAs/InAlAs SPADs [10, 14, 15].

II. DEVICE DESIGN AND FABRICATIONS

In our design, the multiplication layer with thickness of 500 nm is divided into two partitions of 200 nm and 300 nm by an additional charge control layer for obtaining a stepped electric field profile [16]. The electric field distribution within the SPAD device is simulated by using Silvaco Technology Computer Aided Design (TCAD) tools. Fig. 1(a) shows a schematic of the layer structure and Fig. 1(b) the calculated electric fields of the InGaAs/InAlAs SPAD along growth direction respectively at punch-through and breakdown voltage.

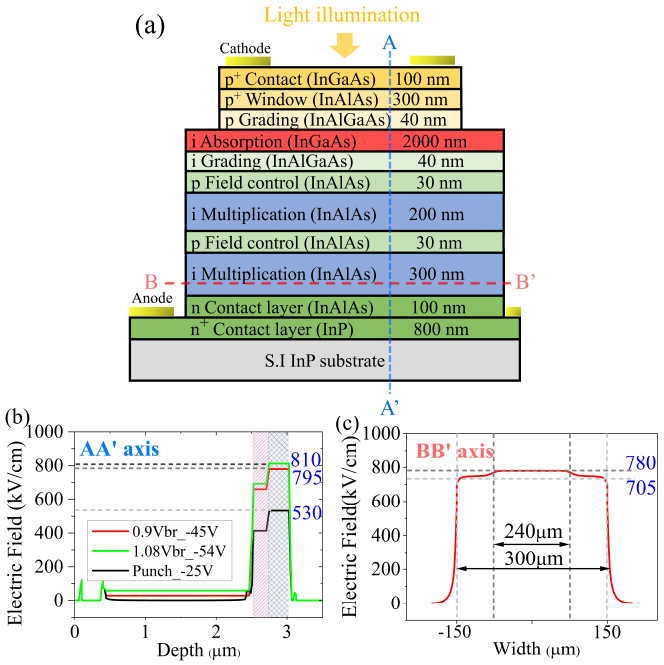

FIGURE 1. **(a) Layer structure of mesa-type InGaAs/InAlAs SPAD. (b) Electric field profile at punch through voltage, 0.9 breakdown voltage and 1.08 breakdown voltage along the vertical direction AA’. (c) Electric field profile for the second (bottom) multiplication layer along lateral direction BB’.**

Due to the stepped electric field profile, the electrons will be energized by the first multiplication layer with thickness of 200 nm, where the electric field strength has not reached the impact ionization threshold, and then transit to the second multiplication layer with the thickness of 300 nm to initiate successive impact ionization. This design provides better localization of impact ionization than can be achieved in uniform multiplication layer of 500 nm, therefore it can reduce the transit time of carrier which governs the timing performance of SPAD. Meanwhile, the occurrence of avalanche events is restricted to the partition of higher electric field strength as indicated by cross-shaded region in Fig. 1(b), which leads to a reduction in the numbers of trap defects so as to reduce the afterpulsing effect. Furthermore, the unique design of the multiplication layer could limit the onset of tunneling within a thinner multiplication layer, therefore it helps to reduce the dark carriers generated via trap-assisted tunneling which dominantly degrade the DCR performance in InGaAs/InAlAs SPADs according to the literature [10].

A double mesa-type SPAD were fabricated to avoid the edge breakdown and to provide a lateral confinement of high electric field as shown in Fig. 1(c), where the terrace of second mesa (with the diameter of 300 μm) surrounding the first mesa (with the diameter of 240 μm) exhibits smaller

strength of electric field. The SPAD structure consists of a 2000-nm-thick InGaAs absorption layer and a 500-nm-thick InAlAs multiplication layer. The first charge control layer ensures the low and high electric fields across the absorption and multiplication layers. The second charge control layer was inserted into the multiplication layer for forming a stepwise electric field distribution. Two grading layers were utilized to reduce the carrier trapping at the abrupt InGaAs/InAlAs heterojunctions. The mesa structures were defined by standard photolithography and formed by wet etching in a $K_2Cr_2O_7$ based solution. The surface of sidewall was treated with ammonium sulfide and followed by a benzocyclobutene (BCB) passivation. Ni-Ge-Au and Ti-Au were used as the Ohmic contact for n^+ InP and p^+ InGaAs layer. The contacts were deposited by e-beam evaporation and alloyed by rapid thermal annealing at 420 °C for 30 s in nitrogen ambient. A final antireflection coating targeted at 1310 nm was deposited on the top of the optical window.

III. EXPERIMENTAL RESULTS AND DISCUSSION

We experimentally characterized the performance of our top-illuminated InGaAs/InAlAs SPAD, with a 240 μm active area diameter, operated in a gated mode with a passive quenching circuit. The gate width is 5 ns. The performance of SPAD was carried out in a LN_2 open-cycle cryostat (Optistat CF, Oxford Instruments) which can cool the device down to 77K. The electrical signals can be applied and taken from the electrical feedthrough of the cryostat. The applied voltage is composed of a dc component and a gate pulse with repetition rate of 10 kHz for DCR and SPDE measurements. The constant dc voltage is set below the breakdown voltage. The excess amount of bias voltage was shown in percentage in this article and the exact values are rescaled according to the breakdown voltage at each temperature.

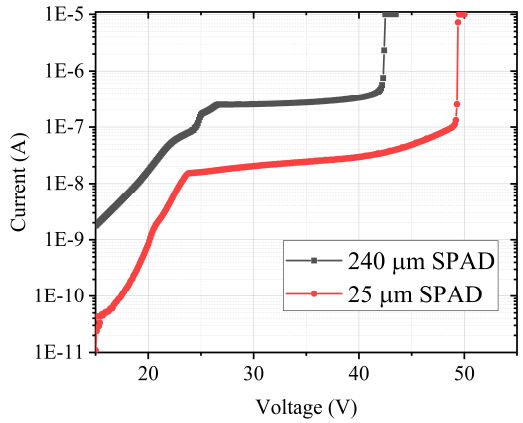

FIGURE 2. **Dark current-voltage characteristic of a 240 μm and 25 μm SPADs at room temperature.**

From the current-voltage I-V characteristics measured at room temperature, which is shown in Fig. 2, the punch-through voltages for large and small devices are about 25 V (large device) and 23 V (small device), which is also examined by the capacitance-voltage characteristics measurement, the breakdown voltages, defined at a dark current of 10 μA, are 42.7 V and 49.7 V, respectively. The temperature coefficient for both devices is 49 mV / K. Note that the difference in the punch-through and breakdown voltages between 240 μm and 25 μm devices can be attributed to 10 % deviation in the doping concentration of top charge control layer between two different wafers. Two wafers were purposely designed to obtain optimal gap between punch through voltage and breakdown voltage for a wide range of operation temperatures and investigation window (around 100 to 300 K) by slightly adjusting the doping concentration of charge control layer. Even though there is a slight difference in the charge control layer between these two devices which could result in different field strength in the absorber, we focus our aim to discuss the effect of stepwise electric field profile on the timing performances of such two devices rather than SPDE.

The dark current of our SPAD is dominantly attributed to the leakage from periphery since the dark current scales with the diameter instead of the area size. Therefore, the dark current is not effectively reduced by shrinking the diameter from 240 μm to 25 μm. Therefore, optimizing the fabrication process in the future, in particular etching and passivation techniques, is instrumental for suppressing the sidewall leakage current. The capacitance-voltage measurement, which is not shown here, exhibits a three step-like decrease with increasing reverse bias. The background doping depletion in InGaAs absorption layer contributes to the initial rapid decrease in capacitance at the reverse bias of 4 V. Then the depletion of top and bottom multiplication regions contributes to the capacitance decrease respectively at 15 V and 26.5 V.

We further characterized the primary DCR per area (normalized to the device area) of two SPADs over a wide temperature range from room temperature to 100 K under different excess bias voltages, which is shown in Fig. 3. The measured dark count rate is converted to an equivalent DCR in free-running mode by considering the duty cycle of gate pulse. For 240 μm SPAD, the DCR at between room temperature to 200 K slightly decreases with temperature. From the slope of DCR curve from 200 K to 300 K, the activation energy of about 0.1 eV was obtained. This value is far smaller than the half of InGaAs bandgap, manifesting that the dominant mechanism of dark carrier generation is tunneling generation, while the thermal generation is not evident. When the temperature is further reduced from T = 187.5 K, DCR increases due to the stronger afterpulsing effect at lower temperature. The minimal DCR for 240 μm SPAD occurs at the temperature of 187.5 K. The DCR curve shows very different temperature characteristics between 25 μm and 240 μm SPAD. For 25 μm SPAD, the DCR arrives at the minimum at T = 125 K, much lower than that of 240 μm SPAD. We fairly attribute the difference in the temperature

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turning point to the ease-up of afterpulsing effect for smaller device, which will be discussed later in Fig. 4.

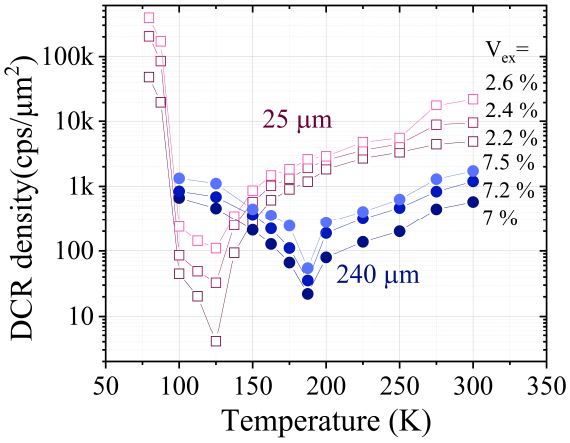

FIGURE 3. **Primary DCR density as a function of temperature for 240 μm (solid symbol) and 25 μm (open symbol) SPADs at various excess bias percentage.**

The afterpulsing effect was characterized through the double-pulse method [17]. A laser pulse was synchronized with the first gate, triggering an avalanche event, and the second "dark" gate is applied for measuring the subsequent avalanche event. Fig. 4 shows the afterpulsing probability as a function of hold-off time for 240 μm and 25 μm SPADs under optimum excess bias and at 200 K. Here the optimum excess bias was chosen for the best SPDE performance and might be different for different devices. The afterpulsing can be reduced to below 1% while operating at the hold-off time of 12.5 μs and 2.8 μs for 240 μm and 25 μm SPADs, respectively. Less afterpusling in the small SPAD is mainly due to fewer number of traps for smaller area size, which explains the difference of the temperature turning point in DCR characteristics between large and small SPADs in Fig. 3.

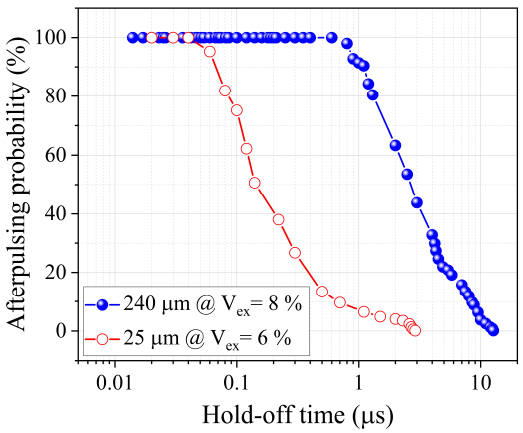

FIGURE 4. **Afterpulsing probability versus the hold-off time at 200 K for 240 μm and 25 μm SPADs.**

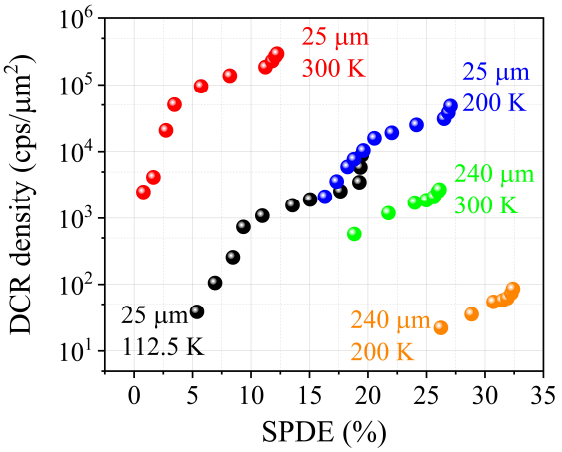

FIGURE 5. **DCR per area versus the SPDE for 240 μm and 25 μm SPADs at various temperatures.**

We perform the SPDE measurement by illuminating the SPAD device with a picosecond laser (Advanced Laser Diode Systems, PiLas131) which produces a light pulse with a width of ~50ps at 1.31 μm. The light pulse is attenuated to about 0.17 photons per pulse. The laser beam coupled through a 9 μm single mode fiber is first collimated. Then the collimated beam is focused by a 10 X NIR objective lens with a long working distance of 3 cm (NA= 0.26) to a spot size of 20 μm well smaller than the active window of both devices to ensure all the photons can be collected. Fig. 5 shows the DCR per area versus the SPDE for 240 μm and 25 μm SPAD at several temperatures. The highest achieved SPDE for 240 μm SPAD is about 32 % under the excess bias of 8 % and at 187.5 K, where the DCR density is about 88 cps/μm^2. For 25 μm SPAD, the SPDE is about 27 % under the excess bias of 6 %, where the DCR density is 48 kcps/μm^2. The SPDE of larger device is higher for that a large area device exhibits more uniform electric field distribution that improves the avalanche triggering probability. The SPDE also shows temperature dependence for both devices. SPDE reaches maximum value at 200 K because the avalanche triggering probability is enhanced when temperature decreases. However, as the temperature is further reduced to 112.5 K, both the thermal energy of electrons and the electric field across the barrier induced by bandgap difference between the absorber and the multiplication layer are reduced, thus the SPDE declines with further reducing temperature [18]. Our proposed structure improves the DCR of small area device for about one order as compared to the reported InGaAs/InAlAs SPADs [10]. However, it is worthy to mention that the DCR cannot be decreased with reducing the area as expected for current production of SPADs, which is due to the high electric field strength existing at the etched sidewall (as shown in Fig. 1(c),) where surface defects (states) concentrates. This leads

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to potentially high DCRs. The surface effect becomes more pronounced in the small device because that the avalanche carriers can more likely reach the sidewall surface. The DCR performance could be improved by introducing a triple mesa with inverted structure to reduce the peripheral electric field strength as proposed in Ref. [19, 20] in order to better control the electric field strength with an edge-field buffer layer. Our SPAD presents remarkable performance even at room temperature, where the SPDE of 240 μm and 25 μm SPAD are respectively 26% and 12%, and the DCR per area are 3 kcps/μm^2 and 290 kcps/μm^2, respectively. To operate SPAD under room temperature is very attractive since it reduces not only the complexity of cooling systems but also the issue of afterpulsing.

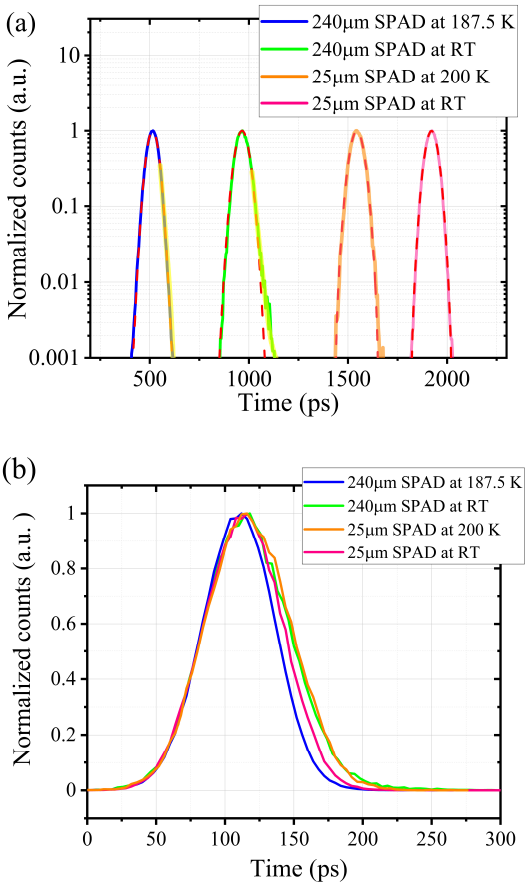

FIGURE 6. (a) **Normalized temporal response distribution for 240 μm SPAD at the excess bias percentage of 8 % for the temperature of 187.5 K and room temperature and that for 25 μm SPAD at the excess bias of 6 % for the temperature of 200 K and room temperature. The red dashed line is the fitted curve with Gaussian distribution function and the yellow pigment is the fitted curve with exponential function. (b) Overlap of temporal response distributions in linear scale.**

Fig. 6 (a) shows the temporal response of 240 μm and 25 μm SPAD measured at the optimum excess bias of 8 % and 6 % respectively. Here we also chose the optimum excess biases for which the best SPDE can be obtained. The temporal response is measured under weak light illumination and enough integration time to avoid the pile-up effect. We also displayed all the temporal responses in linear scale in Fig. 6(b) for a better comparison. The temporal response of both 240 μm and 25 μm SPAD perfectly follows a Gaussian distribution function with FWHM of 60-70 ps and are almost free from exponential tail. Such neat temporal characteristics are very appealing for the applications of time-correlated single photon counting as well as ranging system. More precisely, our SPADs, regardless of the area size, exhibits a narrow full-width at one-thousandth maximum of near 200 ps. Since the FWHM value of SPAD is close to the instrument response limited by the laser pulse width, one can calculate the FWHM of the SPAD jitter by deconvolving the FWHM of laser from the FWHM of the measured waveform. After deconvolution, the actual best jitter of 35 ps is obtained. The temporal response for 240 μm SPAD at room temperature still closely follows a Gaussian distribution function with the FWHM of 72 ps and have only a slight tail with the time constant of 17 ps. The nearly identical temporal characteristics of the 240 μm and 25 μm SPAD demonstrate that the lateral avalanche propagation is not the dominant mechanism in determining jitter for these devices. The tail-less response indicates that both the lateral drift and longitudinal diffusion is eliminated. The temporal response with nearly tail-less characteristic is better than that has ever been reported for InGaAs/InP SPADs and InGaAs/InAlAs SPADs [10,14,15], where their temporal responses usually have a main peak accompanying with a slow tail. To our knowledge, the best full width at 1/1000 of the maximum of 360 ps were reported by Ref. [21]. Table 1 lists several figure of merits of other reported SPADs as well as our SPADs for a better comparison. Note that all the figure of merits were recorded under the excess biases for which the best SPDE can be obtained. The measured DCR density for 240 μm SPAD is comparable to the reported value of InGaAs/InP SPAD [15] and better than the recent published results of InGaAs/InAlAs SPAD [9, 10]. Both the DCR and SPDE can be further improved by a delicate fabrication process to efficiently eliminate the edge breakdown. Nevertheless, we believe that this novel concept can be also applied to the InGaAs/InP based SPADs and could achieve a breakthrough in their performance.

TABLE I
FIGURE OF MERITS OF OUR AND OTHER SPADS

	InGaAs/InAlAs SPAD					InGaAs/InP SPAD	
	This work				X. Meng et. al. [9]	A. Tosi et. al. [15]	M. Liu et.al. [16]
Diameter (μm)	240		25		25	25	40
Temp. (K)	300	187.5	300	200	210	225	200
DCR (Hz/μm²)	3000	88	3×10^5	5×10^4	2×10^5	14	10
DCR (cps)	2×10^8	5×10^6	2×10^8	3×10^7	1.3×10^8	8.8×10^3	1.2×10^4
SPDE (%)	26.3	32.3	12.2	27.1	26	37	45
FWHM (ps)	72(52)	61(35)	67(45)	73(53)	70	87	140
FW(1/1000)M	274	212	204	204	-	360	~400

IV. CONCLUSION

In this paper, we designed and demonstrated both large and small InGaAs/InAlAs SPADs, achieving reasonable DCR, moderate SPDE, and state-of-the-art neat temporal performance, which is especially promising for time-resolved measurements and TOF measurements demanding low noise, high detection efficiency and picosecond timing accuracy. SPAD with large active area is exploitable for an SPAD array, profiting optical communication as well as scanning LiDAR systems. In our work, if the sidewall can be better treated, smaller SPAD dimension can reduce the DCR, timing jitter and afterpulsing and also enables a higher dynamic range for array applications. The performance of our SPAD can be further improved by using advanced quenching techniques or by integrating monolithically with a passive resistor. Our approach provides a strategy in designing a large area SPAD of excellent temporal performance without losing its detection ability and can be easily applied to other material system.

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