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$In_{0.52}Al_{0.48}As$ Based Single Photon Avalanche Diodes with Stepped E-field in Multiplication Layers and High Efficiency Beyond 60 %

Yi-Shan Lee, Yan-Min Liao, Ping-Li Wu, Chi-En Chen, Yu-Jie Teng, Yu-Ying Hung, Jin-Wei Shi

***Abstract*—We carry out an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ single photon avalanche diode which exhibits a single photon detection efficiency exceeding 60% at 1310 nm and neat temporal characteristic of 65 ps. A novel concept of dual multiplication layer is incorporated to avoid the tradeoff between dark count rate, afterpulsing and timing jitter, paving the possibility to improve the overall performance of a single photon detector. Based on this elevated device structure, we further optimize the detection efficiency and timing jitter by employing a delicate mesa structure to better confine the electric field distribution within the central multiplication region. For our detector operated under gated mode, a shorten gate width together with an increase of excess bias percentage leads to a significant improvement in the detection performance. We eventually achieve a single photon detection efficiency of 61.4% without the involvement of afterpulsing at the gating frequency of 10 kHz for 200 K.**

***Index Terms*—Single photon avalanche diode, photon detection efficiency, timing jitter**

I. Introduction

SINCE single photon detector (SPD) offers the ultimate sensitivity, it facilitates the fast development of quantum information technologies [1]. Variety of applications such as light detection and ranging (LiDAR) and time-resolved single molecule spectroscopy also benefits from the supreme sensitivity and picosecond temporal response of SPD [2, 3]. Single photon avalanche diode (SPAD) stands out among other SPDs thanks to the advantages of their compactness, cryogenic-free operation and low cost. Extending the spectral range to short-wave infrared (SWIR) region provide the compatibility of SPAD with fiber-based applications and also permit higher optical power at eye-safety threshold for the LiDAR applications. The single photon detection performance of SPAD is characterized by several figure of merits, dark count rate (DCR), single photon detection efficiency (SPDE), maximum count rate, afterpulsing probability and timing jitter. SPADs of high SPDE and low DCR are especially favored in numbers of applications such as quantum key distribution and a range of time-correlated single photon counting (TCSPC) measurements. In the SWIR region, compared with $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ SPADs, the $In_{0.53}Ga_{0.47}As/InP$ SPADs have received more research interests over the past decade due to the improved epitaxy and fabrication techniques [4-9]. However, $In_{0.52}Al_{0.48}As$-based APDs are increasingly being studied instead of InP-based APDs as they exhibit superior performance due to the large difference between the electron and hole ionization coefficients which contributes to a low excess noise, high gain-bandwidth product and better sensitivity upon $In_{0.52}Al_{0.48}As$-based APD. Moreover, in light of larger bandgap, high-electron mobility and less temperature dependence of ionization coefficient ratio, the detection performance of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ SPAD can be improved in terms of breakdown, temporal and temperature characteristics, which appears to be the next choice for the upcoming decade of solid-state SPD development [10-13].

The first $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ SPAD was reported by Karve et al. [14]. They have demonstrated a SPAD with SPDE of 16 % at 130 K. Nakata et al. further improved the overall performance with SPDE of 10 % at 213 K [15]. In addition, Zhao et al. has designed an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ SPAD with SPDE of 6 % and 14 % at respective 240 K and 120 K based on the self-quenching and self-recovering mechanism [16]. More recently, Meng et al. demonstrated a mesa-type $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ SPAD with SPDE of 21 % at 260 K [17]. By further increasing the thickness of absorption and multiplication layer to the respective thickness of 1700 nm and 1000 nm, they achieved SPDE of 26 % and DCR of 100 MHz at 210 K [18]. Very recently, Zhang et al. incorporated a triple mesa structure to suppress the surface leakage current, achieving SPDE of 35 % and DCR of 33 MHz at 240 K [19]. However, for the above reported $In_{0.52}Al_{0.48}As$ -based SPADs, the DCRs remain several orders higher compared with the InP-based SPADs. It is the tunneling current from the $In_{0.52}Al_{0.48}As$ multiplication layer that hinders the efficient DCR suppression during cooling. In order to reduce the tunneling current, the thickness of multiplication layer should be increased to avoid the direct-tunneling generation. However,

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with thicker multiplication layer, the accompanying issues of broadened temporal distribution and afterpulsing effect emerge.

By incorporating a unique structure design, our previous report on $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ SPAD, which consists of a dual multiplication layer with an overall thickness of 500 nm, have achieved the best SPDE of 32 % and 26 % respectively at 187.5 K and room temperature with a moderate DCR of 200 MHz and 5 MHz [20], though it still falls behind the superb SPDE exceeding 60 % from recently reported InGaAs/InP SPADs [21-23]. In our previous work, the DCR originated from the high periphery electric field existing at the etched sidewall is the main obstacle to achieve higher SPDE. Therefore, in this work, we modify the mesa structure in order to reduce the periphery electric field and have stronger confinement of the high electric field within the center of active mesa. Meanwhile, we shorten the gate width to reduce the DCR and hence avoid the count rate saturation when the excess bias is further raised to boost the SPDE. By combining the above improvement in fabrication and gate operation, we achieve SPDE as high as 61.4 %, which is, to our knowledge, the best among the reported In0.53Ga0.47As/In0.52Al0.48As SPADs at 1310 nm and comparable to the reported In0.53Ga0.47As/InP SPADs at 1550 nm for the same thickness of 2-μm InGaAs absorption layer. Such high SPDE is obtained at the cost of relatively high DCR performance. Based on our current structure with high responsivity (larger than 1 A/W), the applications using time-gated strategy is ambitiously envisioned for that the synchronization of the gated signal of SPAD with incoming single-photon data stream can mitigate the problem of high DCR in our device [24].

II. STRUCTURE DESIGN AND EXPERIMENTAL DETAILS

The avalanche triggering probability highly depends on the multiplication region width, electric field, excess bias and temperature. Thicker multiplication region can increase the avalanche triggering probability and reduce the DCR, but at the cost of poor temporal and speed performance. When the thickness of multiplication layer is reduced to improve the temporal characteristic and operation speed of SPAD, the tunneling effect and dead space effect become more pronounced [9]. The avalanche triggering probability increases faster with excess bias ratio when the dead space occupies a larger fraction of the multiplication region width [25], however, the tunneling generation also begins to dominate the bulk current prior to the avalanche breakdown, imposing an upper limit on the bias voltage range for the SPAD with thin multiplication layer [10].

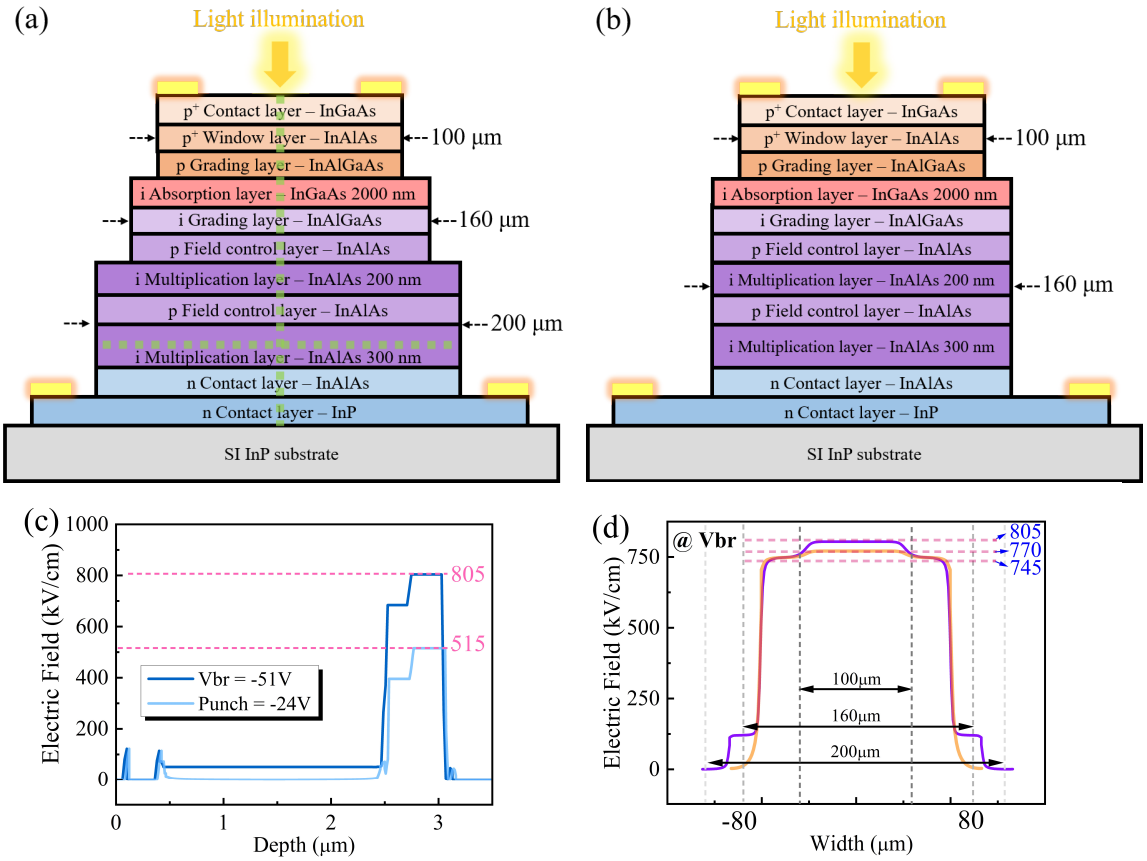

Fig. 1. Fig. 1. Illustration of layer structure and etching profile for InGaAs/InAlAs SPAD with (a) quadruple mesa structure and (b) triple mesa structure. (c) Electric field profile at punch through and breakdown voltage along the vertical growth direction as indicated by the longitudinal green dashed line in (a). (d) Lateral electric field profile at the second (bottom) multiplication layer (along the transverse green dashed line in (a)) for triple (orange) and quadruple (purple) mesa structures.

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Our design concept aims at circumventing the trade-off between DCR induced by tunneling generation, afterpulsing (maximum count rate) and timing jitter. Therefore, we propose a SPAD structure with a relatively thin multiplication layer as compared to a normal SPAD structure which usually consists of at least 1000-nm-thick multiplication layer. The layer structure of our SPAD device is detailed in Fig. 1(a). The wafer was grown by molecular beam epitaxy (MBE) on a semi-insulating InP substrate. A 2000-nm-thick absorption layer is designed for increasing the photon absorption efficiency. Two grading layers are used to reduce the carrier accumulation at the abrupt $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterojunctions. The doping concentration of top field control layer is properly chosen to ensure a low but high enough electric field strength in the absorption layer for drifting the photogenerated carriers to the multiplication layer. With inserting an additional bottom field control layer, a 500-nm-thick multiplication layer in a conventional separate absorption, grading, charge and multiplication (SAGCM) structure is partitioned into a 200-nm-thick top multiplication layer and a 300-nm-thick bottom multiplication layer. A stepwise electric field distribution in the growth direction is thus formed in the multiplication layer as shown in Fig. 1(b), where the electric field distribution is calculated by using the Silvaco Technology Computer Aided Design (TCAD) tools. The electric field strength in the top multiplication layer with the thickness of 200 nm, which has not reached the threshold of impact ionization, will energize and accelerate the carriers to the bottom multiplication layer. The carriers entering the bottom multiplication layer with the thickness of 300 nm will trigger subsequent impact ionizations, creating a self-sustaining avalanche. The top multiplication layer in our design can act to build up the initial energy of all the carriers and align them at the same starting point, which in principle can minimize the dead space effect and maintain the applied bias voltage range while reducing the thickness of multiplication layer.

Based on our previous work, this design has been proven to provide an excellent timing performance with considerable improvement in the DCR as compared with other reported $In_{0.52}Al_{0.48}As$ SPADs [20]. We continue to put effort on the optimization of SPAD performance from the aspect of fabrication processes. As mentioned previously, since the avalanche triggering probability depends on the electric field distribution, we incorporate a quadruple mesa configuration to better confine the high electric field within the central active multiplication region. The etching profile for the quadruple and triple mesa is illustrated respectively by Fig. 1(a) and Fig. 1(b). The photo-active area with the diameter of 60 μm is defined by the first mesa with the diameter of 100 μm and surrounded by the second and third mesa with the diameter of respective 160 μm and 200 μm. The lateral electric field distribution of bottom multiplication region for the quadruple and triple mesa is calculated and shown in Fig. 1(c). As can be seen, the additional second mesa in quadruple mesa device, which is etched through the first field control (charge) layer and stops at first multiplication layer, can more effectively constrain the E-field below it [26, 27]. We can clearly see from Fig. 1(d), as expected, that the electric field reduces from 750 to 90 kV/cm at the sidewall of the second multiplication layer in the quadruple mesa device. The much smaller electric field strength in the edge of multiplication region than that of the triple mesa one can prevent the edge breakdown by well-concentrating the high field region below the first active mesa.

The mesa etching was performed by using plasma dry etching, which is composed of CH_4 and O_2 gas. Since the aluminum based alloy has slower etching rate, the etching depth can be precisely controlled, which ensures a perfect etching stop at first M-layer.

After mesa etching, the surface sidewall was treated with ammonium sulfide and followed by a polyimide passivation. Ni-Ge-Au and Ti-Au were used as the Ohmic contact metal for n^+-InP and p^+-InGaAs layer. The contacts were deposited by e-beam evaporation and alloyed by rapid thermal annealing. In order to optimize the quantum efficiency, a final antireflection coating targeted at 1310 nm was deposited on the top of the active window.

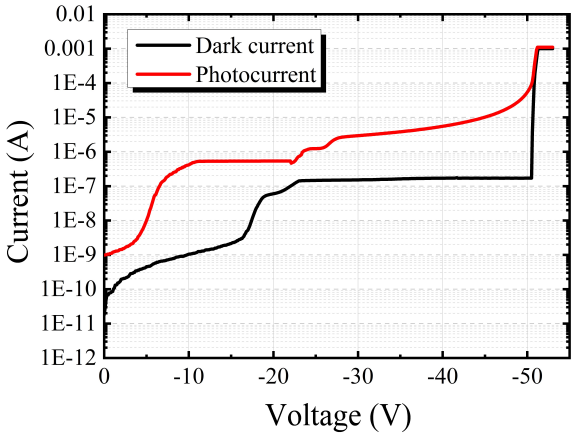

Fig. 2. Dark and illuminated current-voltage characteristics of mesa-type InGaAs/InAlAs SPAD. The SPAD was illuminated with an optical power of 1μW.

The dark and illuminated current-voltage characteristics of our $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ SPAD with specific design are shown in Fig. 2. The punch-through and breakdown voltages are obtained to be respectively 24 V and 51 V, where the breakdown voltage is defined at a dark current of 10 μA. A lensed fiber laser with spot size of 2.6 μm and the wavelength of 1550 nm is used to illuminate the SPAD device. Under the pump power of 1 μW, a maximum responsivity of 1.12 A/W at unity gain is achieved, corresponding to an external quantum efficiency (EQE) exceeding 100 %, which suggests that all the absorbed photons are detected. Therefore, under the estimated EQE and optimized conditions, we can anticipate that the maximum achievable SPDE approaches 100 %. The temperature dependency of the breakdown voltage is 51 mV / K, about half of that obtained from $In_{0.53}Ga_{0.47}As$/InP SPADs [22].

The SPAD is operated under a gated mode with a passive quenching circuit. The applied voltage is composed of a dc

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component and a gated electrical pulse. The constant dc voltage is set below the breakdown voltage. The gate frequency of the electrical pulses for subsequent characterization is 10 kHz. The main gate width of 1.5 ns is used for most characterizations. The SPDE measurements adopting both the gate width of 1.5 ns and 5 ns for showing the significant increase of SPDE due to an increased excess bias percentage. All the characterizations are carried out in a LN2 open-cycle cryostat (Optistat CF, Oxford Instruments) which can cool the device down to 77K. The electrical signals can be applied and taken from the electrical feedthrough of the cryostat. The excess amount of bias voltage shown in percentage in this article is the ratio of excess bias voltage versus breakdown voltage. The excess electric field are guaranteed to be consistent for different temperature by the recalculation of exact dc voltage and gated pulse according to the breakdown voltage measured at every temperature. For illuminated experiments, we use a 1310 nm laser with pulse width of 50 ps at a repetition rate of 10 kHz synchronized with the gate frequency. The laser pulses are attenuated to about 0.17 photons per pulse. The timing jitter is determined by a time-correlated single photon counting module (TCSPC) with a timing resolution of 4 ps.

III. Results and Discussions

The maximum operation speed limited by the afterpulsing effect is characterized via the double pulse method [28]. A laser pulse was synchronized with the first gate, triggering an avalanche event, and the second "dark" gate is applied with an adjustable hold-off time for measuring the correlated avalanche events. We vary the operating temperature at the gate width of 5 ns and 1.5 ns and measure the afterpulsing probability at several selected SPDEs. Fig. 3(a) shows the afterpulsing probability as a function of hold-off time for the gate width of 5 ns. Under this gate condition, the hold-off time required to reduce the afterpulsing probability below 1 % is 5 µs and 0.3 µs respectively at 200 K and 300 K, corresponding to the operation speed of 200 kHz and 3.3 MHz. Furthermore, the afterpulsing probability increases slightly with higher excess bias or with higher SPDE, where the value of SPDE behind the excess bias percentage in the legend is the data measured at 200 K. When the pulse width is reduced to 1.5 ns, the narrower pulse decreases the amounts of carriers generated during an avalanche breakdown event, leading to less pronounced afterpulsing effect. As shown in Fig. 3(b), the afterpulsing probability is greatly decreased as compared to that measured under the gate width of 5 ns. The hold-off time required for minimal afterpulsing probability (1 %) is between 0.02 µs and 0.03 µs when the temperature is changed from 300 K to 200 K, corresponding to the maximum operation speed between 50 MHz and 33 MHz. At 200 K, with the increase of SPDE, the afterpulsing probability exhibits no significant increase. For T= 225 K and 300 K, the afterpulsing probability increases slightly for the excess bias increasing from 9.3 % to 10.5 % (SPDE from 27 % to 61 %). Again, the SPDE in the legend is referred to the data measured at 200 K. Reducing the gate width avoids the afterpulsing effect but also decreases the amplitude of avalanche signal, which makes more difficult to distinguish the avalanche signal from the capacitively-coupled spurious signal. As a result, the level of applied excess bias is elevated and ranges between 7.5 % to 11 % for the narrower gate operation, where the DCR saturation sets the upper limit on the excess bias.

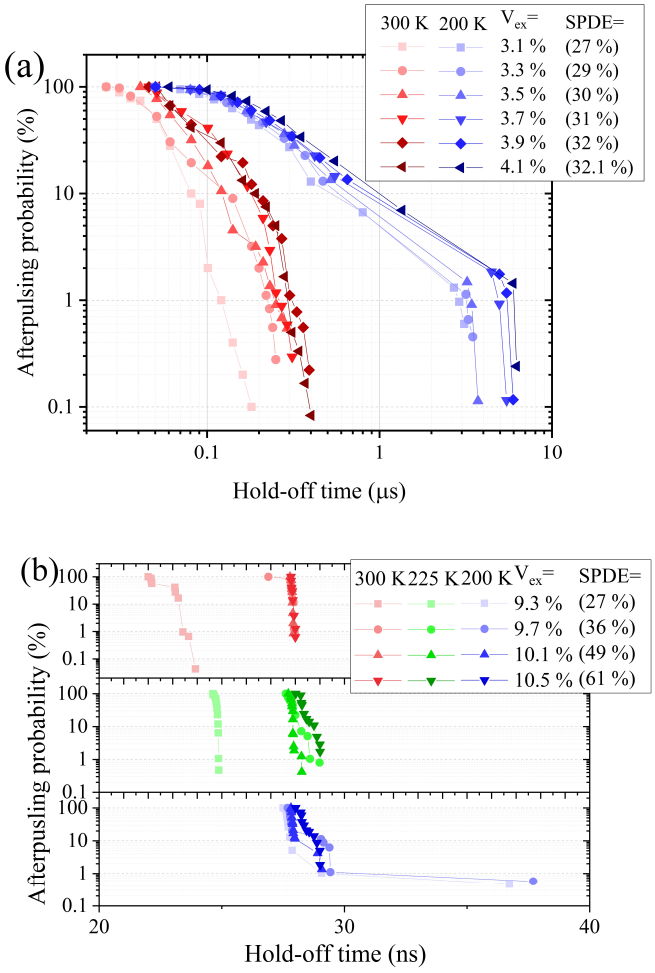

Fig. 3. Afterpulsing probability versus the hold-off time at various temperatures and excess biases for the gate width of (a) 5 ns and (b) 1.5 ns. Different excess bias is applied according to the color scale. The SPDE value measured at 200 K is shown in the parenthesis.

We characterize the DCR and SPDE at the temperature of 200 K and 300 K and at a fixed gate frequency of 10 kHz where the afterpulsing effect can be disregarded through the above examination on the afterpulsing performance. Fig. 4 shows the SPDE versus DCR density (normalized to the area of active window) for triple and quadruple mesa devices at the gate width of 5 ns and 1.5 ns. For the triple mesa device measured at the longer gate width of 5 ns, the highest achieved SPDE for 200 K and 300 K is respectively 24 % and 15 %. The SPDE is notably improved to 32 % and 31 % respectively for 200 K and 300 K due to the enhanced avalanche triggering probability by incorporating a quadruple mesa structure. In particular, for 300 K, a more significant increment of SPDE is observed. For the quadruple mesa devices, SPDE has less temperature dependence, which implies that more uniform and well

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concentrated electric field distribution can offset carrier cooling subjected to the increased phonon scattering at high temperatures. To operate SPAD at room temperature is very attractive since it reduces not only the complexity of cooling systems but also avoid the afterpulsing effect. In addition to the SPDE, the DCR density for quadruple mesa device is several times lower compared to the triple mesa device at the same SPDE.

The highest SPDEs are obtained by reducing the gate width to 1.5 ns in conjunction with higher excess bias. As shown in Fig. 4, the maximum achievable SPDE reaches 61.4 % with 180 kcps/μm^2 DCR at 200 K and even reaches 47 % with 177 kcps/μm^2 DCR at 300 K. Here, the achieved SPDEs (61.4 % at 200 K and 47% at 300 K) is the highest ever reported in InP and $In_{0.52}Al_{0.48}As$ based SPADs [19, 23]. In order to study the possible origins of dark counts, we probe the DCR at various temperatures. The activation energy can be obtained by fitting the ln(DCR) versus 1/kT characteristics, as shown in the inset of Fig. 4. For the longer gate width with lower excess bias, the activation energy is 0.15 eV at the linear fitting range between 200 K and 300K. With a shorten gate width and higher excess bias, the activation energy of 0.06 eV is deduced from the data between 250 K and 300 K. The activation energy far less than the half of energy bandgap of InGaAs layer for both operation conditions suggests that the dark counts is dominantly originated from the tunneling-related generation in the multiplication layer instead of the Shockley-Read-Hall generation in the absorption layer. For the operation with the gate width of 1.5 ns, the tunneling-related generation gets more serious due to the application of higher excess bias. Therefore, for future advanced structure design, the tunneling generation remains the most concerning issue.

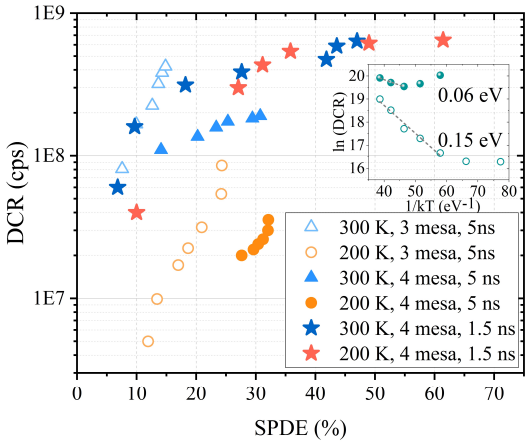

Fig. 4. DCR versus SPDE for triple and quadruple mesa devices at different gate width operations and the temperature of 200 K and 300 K. The inset shows the Arrhenius plot of DCR for the gate width of 1.5 ns (solid symbol) and 5 ns (open symbol). The activation energy can be calculated from the slope of the Arrhenius plot.

The temporal response of our SPAD perfectly follows a Gaussian distribution function and is almost free from the slow diffusion tail [20]. The full-width of half-maximum of Gaussian function, known as the timing jitter, is recorded as a function of excess bias at different operation conditions respectively for the temperature of 200 K and 300 K. Fig. 5(a) shows the changes of the jitter with excess bias. For all operation conditions, the timing jitter universally decreases with increasing the excess bias. In addition, as shown by the data obtained at the gate width of 5 ns, the timing jitter can be greatly improved under the same excess bias by incorporating a quadruple mesa structure. Fig. 5(b) shows the near-Gaussian temporal responses measured at the excess bias of 4.1 %, the gate width of 5ns and T= 200 K respectively for quadruple and triple mesa device. With reducing the gate width and higher excess bias, the timing jitter is no further decreased due to the limitation of instrument response.

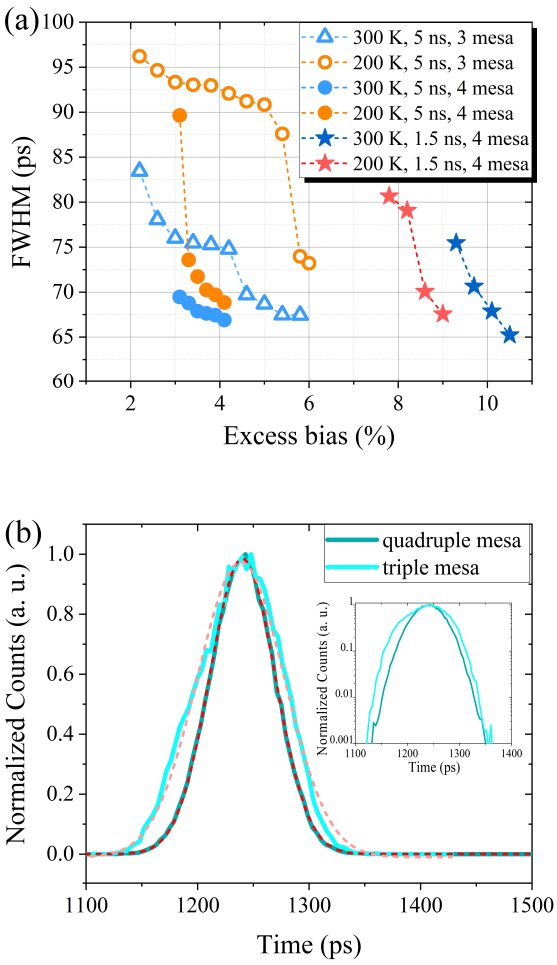

Fig. 5. (a) Timing jitter versus excess bias for quadruple and triple mesa devices at different gate width operations and the temperature of 200 K and 300 K. (b) Gaussian-like temporal responses measured at V_{ex}= 4.1 %, 5ns gate width and T= 200 K for quadruple and triple mesa devices. The red and pink dashed line are the Gaussian fit curves for quadruple and triple mesa devices, respectively. The inset shows the semilog plot of temporal response distributions.

The recent achievement of InGaAs based SPAD has been summarized into Table 1 which lists several figure of merits of SPAD. All the figure of merits are recorded under which the peak SPDE is obtained. The SPDE reported in this work is

better than the recent published results of InGaAs/InP SPAD [22, 23] and InGaAs/InAlAs SPAD [19], however, at the cost of relatively high DCR. Further improvement in the device DCR performance can be expected by only slightly increasing the thickness of multiplication layer to reduce the tunneling generation.

IV. Conclusion

We have demonstrated an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ SPAD with high SPDE beyond 60 % at 1310 nm. By introducing a distinct design of dual multiplication layer, we overcome the trade-off barrier that exists between the DCR, afterpulsing effect and the timing jitter. The highest EQE of over 100 % was achieved based on the optimization of vertical electric field. The lateral electric field distribution is more uniform and well concentrated by incorporating a quadruple mesa structure. The advanced device structure in conjunction with a shorten gate width, the SPDE, an important figure of merit for SPADs, reaches 61.4 % with 180 kcps/μm^2 DCR at 200 K without the involvement of afterpulsing effect. Our detector featuring a high efficiency detection of near-IR photons and low jitter is desired especially for the outdoor direct time-of-flight LiDAR and enables the extension from short- to long-range.

TABLE I FIGURE OF MERITS OF OUR AND OTHER SPADS

	Material	**Diameter (μm)**	**V_{ex}/V_{BD} (%)**	**Peak SPDE (%)**	**DCR density (cps/μm^2)**	**Jitter (ps)**	**Diffusion tail (ps)**	**Temperature (K)**
Tosi [9]	InGaAs/InP	25	15	37	24	87	360	225
Liu [5]	InGaAs/InP	40	6	45	7.5	140	400	200
Comandar[22]	InGaAs/InP	--	14	55	--	91	--	293
Fang [23]	InGaAs/InP	25	27	60	5.4×10^2	--	--	300
Zhang [19]	InGaAs/InAlAs	25	3	35	5.3×10^4	--	--	240
Our previous work [20]	InGaAs/InAlAs	240	8	32.3	87	61	N/A	187.5
This work	InGaAs/InAlAs	60	8.3	61.4	1.8×10^5	65	N/A	200

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