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High-brightness and high-speed vertical-cavity surface-emitting laser arrays

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High-power vertical-cavity surface-emitting laser (VCSEL) arrays, which can serve as the light source in modern lidar and three-dimensional optical sensing systems, have recently attracted a lot of attention. In these types of systems, the time-of-flight (ToF) technique, based on the round-trip time of short optical pulses is usually adopted. Further enhancement of the ranging distance and depth resolution in these ToF driven systems by the incorporation of a VCSEL array with a high available power, high brightness (narrow divergence angle), and fast response time is highly desirable. However, a large number of light emission apertures (several hundreds) in the VCSEL array is usually necessary to raise the output power level to several watts. This leads to a large parasitic capacitance and the RC-limited bandwidth may become the dominant limiting factor of the speed of the high-power VCSEL array. In this work, Zn-diffusion and oxide-relief apertures are used to manipulate the optical modes and reduce the parasitic capacitance, respectively, in a unit device for a 940 nm VCSEL array. The demonstrated VCSEL array has a quasi-single-mode output, high available power (4 W; 1% duty cycle), narrow divergence angle (∼14° at $1/e^2$) under maximum output power, and a fast rise time (<100 ps). These results open up new possibilities for further enhancing the performance of ToF sensing systems at the 940 nm wavelength.

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1. INTRODUCTION

The development of lidar has recently seen great advancement, especially for use in autonomous cars, robots, and unmanned aerial vehicles, anywhere it is necessary to monitor both fast moving and fixed objects in real time. Three-dimensional (3D) lidar plays a critical sensing role to attain this goal [1]. To date, most of the commercially available lidar systems incorporate direct detection time-of-flight (ToF) sensors operating at 905 or 940 nm [1,2]. In such lidar systems, high-power (> watts output power) vertical-cavity surface-emitting laser (VCSEL) arrays [2–5] or high-power distributed feedback (DFB) lasers [2,6] can serve as the light sources. Compared with the DFB lasers, the VCSEL array has the advantage of lower fabrication cost and easier mass production [2]. Nevertheless, the optical design for the VCSEL array driven ToF system is more difficult than that of a DFB-based system with a single cavity due to the fact that the VCSEL array is comprised of hundreds of light emission apertures (cavities) and usually cannot sustain stable single-lobe far-field patterns (FFPs) (single spatial mode) under the full range of bias currents [2], which results in a large divergence angle (25°–30° at $1/e^2$), and lower brightness of the output optical beam. In addition, for ToF applications, the VCSEL array chip usually needs to be integrated with a holographic diffuser and a high-brightness VCSEL light source can further enhance the contrast ratio at the boundary of the far-field pattern output from the whole integrated module [7]. An extended ranging distance can also be expected. The modulation speed of the light source also plays an important role in determining the depth resolution of the lidar and 3D sensing system. There is a trade-off between the output power and 3 dB electrical-to-optical (E-O) bandwidth performance in the VCSEL array since its output power is proportional to the total light emission active area. A larger active area is always accompanied by larger parasitic and junction capacitances, which in turn degrades the RC-limited and net E-O bandwidths of the VCSEL array. By optimizing the VCSEL-to-VCSEL spacing, mesa shape, emitting diameter, and number of emitters, improved high-power (∼50 mW) and high-speed (∼25 GHz) performance of small-scale (seven elements) 980 nm VCSEL arrays has been successfully demonstrated [8]. However, in order to achieve several watts of output power, hundreds of light emission apertures are necessary, which results in enormous parasitic capacitance in high-power VCSEL arrays. In order to attain the desired RC-limited bandwidth in such a large array, the proper value of inductance, which is induced by the bond wires in the VCSEL array package, is necessary [2,9]. A rise time of 300 ps

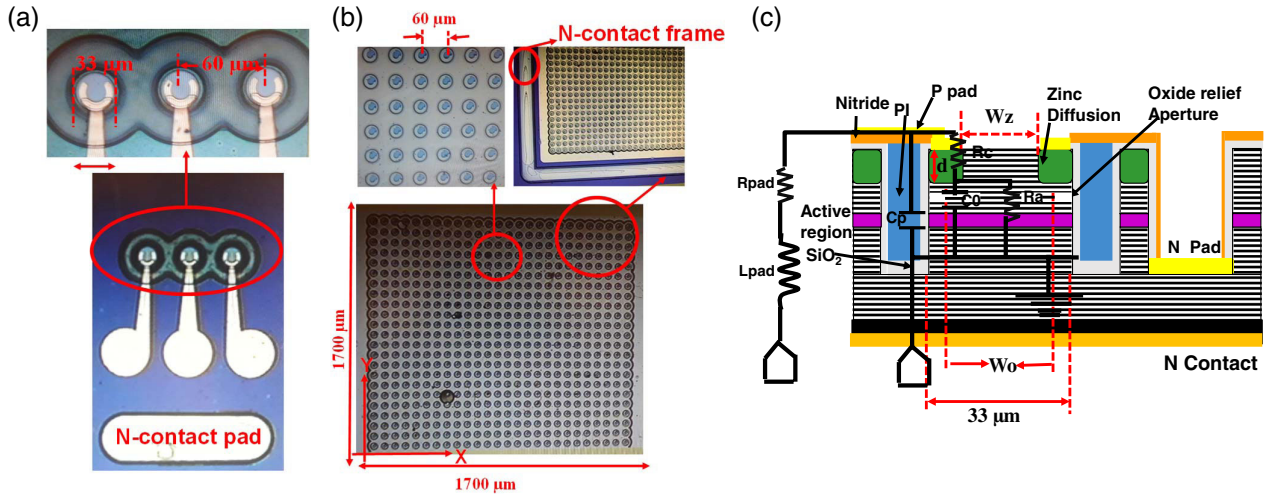

Fig. 1. Top view of the (a) single reference VCSEL unit, (b) VCSEL array, and (c) conceptual cross-sectional view of the VCSEL unit with the corresponding equivalent-circuit model of the demonstrated device ($W_o/W_Z/d$: 9.5/7.5/1.7 μm).

is usually feasible for a high-power VCSEL array having a packaged inductance of less than 0.3 nH under a 5 A driving current [2]. In order to release the limitation on bond wire inductance (lengths), it is highly desirable to greatly reduce the parasitic capacitance in a high-power VCSEL array [9]. In previous work [10–15], Zn-diffusion and oxide-relief techniques were used to reduce the differential resistance and parasitic capacitance of VCSELs, respectively. The single 940 nm VCSEL demonstrated a record-high 3 dB E-O bandwidth (40 GHz) [13] and elimination of the bandwidth degradation in a small-scale 850 nm VCSEL array (three elements) as compared to a single [12]. In this work, for the first time, the Zn-diffusion and oxide-relief techniques are utilized to stabilize the output far-field patterns of high-power (several watts) VCSEL arrays for narrow divergence angles and reduce the parasitic capacitance, respectively. Compared to the ultra-fast 940 nm VCSEL reported in our previous work [13], the VCSEL epi-layer structure here has been greatly modified for parallel connection of hundreds of light emission apertures and high-power performance. These VCSEL arrays demonstrate stable quasi-single-mode (QSM) output under the full range of bias currents, with a high available maximum power (4 W; 1% duty cycle), narrow divergence angle (∼14° at $1/e^2$ under maximum output power, and fast rise time (<100 ps). Compared to the performance of commercially available high-power VCSEL array chips operating at the same 940 nm wavelength [16], the demonstrated VCSEL array can achieve a 10 times faster rise time (0.1 versus 1 ns), single-spot far-field distribution (doughnut free), narrower $1/e^2$ divergence angle (14° versus 25°), and comparable static light output power–current–voltage (L-I-V) performances (>2 W output under 3 A bias current). The excellent characteristics of the device show how the Zn-diffusion and oxide-relief techniques can effectively improve the performance of large-area (>1 mm^2) and high-power VCSEL arrays in terms of the modulation speed and far-field patterns. The results also open up new possibilities to further enhance the depth resolution in infrared (∼900 nm) ToF lidar systems.

2. VCSEL ARRAY STRUCTURES

In order to characterize and evaluate the performance of our VCSEL array, some single VCSEL units were also fabricated along the array. Figures 1(a)–1(c) show top views of the demonstrated single reference VCSEL and VCSEL array, and a conceptual cross-sectional view of the VCSEL unit, respectively. As can be seen in Fig. 1(a), three of the single VCSELs share the same n-metal pads. The mesa size (W) and the spacing between neighboring VCSEL units (D) in the 1 × 3 column are the same as those of the VCSEL unit in the array, which has a W and D of 33 and 60 μm, respectively. These two parameters are specified in Figs. 1(a) and 1(b). The total number of light emission apertures in our array is around 570 with a 1.7 mm × 1.7 mm active area. For both the single device and the array, the *n*-type contacts on the bottom side of the *n*-type GaAs substrate ensure uniformity of the current distribution in each light emission aperture. Furthermore, for the benefit of on-wafer high-speed measurement, an extra *n*-contact frame surrounds the light emission apertures on the top side of our array. As shown in Fig. 1(c), there are three key parameters: W_Z, W_O, and d, which determine the mode characteristics of the single device. Here, W_Z and W_O represent the diameter of the Zn-diffusion aperture and oxide-confined aperture, respectively; d is the Zn-diffusion depth. The addition of Zn-diffusion apertures in the top *p*-type distributed Bragg reflector (DBR) layers of our VCSEL will induce extra loss in the peripheral region of an optical aperture. Higher-order mode lasing can thus be suppressed in the Zn-diffused DBR region due to free-carrier absorption and reflectivity reduction caused by disordering [10–15]. The disordering of the DBR layers allows us not only to manipulate the number of optical transverse modes inside the VCSEL cavity, as discussed elsewhere, but can also reduce the differential resistance of the VCSEL [10–15]. By properly optimizing the relative sizes of these three parameters to let a significant Zn-diffusion-induced internal loss (α_i) happen in the current-confined (gain) region, the device is able to demonstrate high single-mode (SM) performance under the full range of bias currents in a 10 × 10 VCSEL array [14].

However, high SM performance is usually accompanied by a significant increase in the threshold current due to the increase of α_i. For such a large array, the amount of operating current and its induced device heating play crucial roles in array performance. Here, the geometric sizes of W_o, W_z, and d are chosen to allow both the single reference device and array to have quasi-SM performance over the whole range of bias currents, low I_{th} (0.7 mA

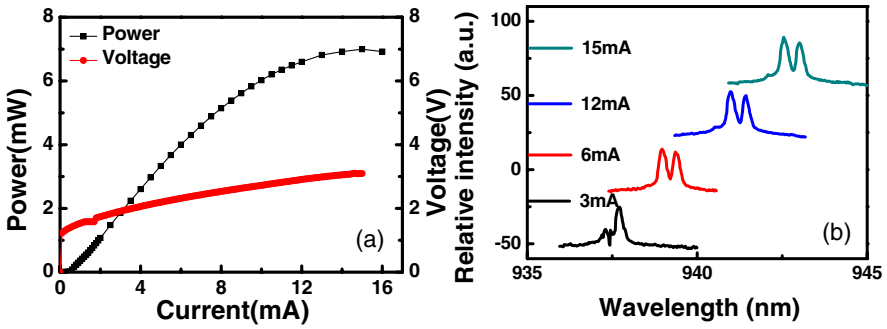

Fig. 2. (a) Measured L-I-V curve of a single VCSEL unit, (b) measured optical spectra of a single VCSEL unit at different bias currents ($W_o/W_Z/d$: 9.5/7.5/1.7 μm).

for the single device), and high output power (7 mW for the single device). Their values ($W_o/W_Z/d$: 9.5/7.5/1.7 μm) are specified in Fig. 1.

The epi-layer structure is composed of three compressive strained $In_{0.3}Ga_{0.7}$ As/$Al_{0.37}Ga_{0.63}$ As (4/8 nm thickness) multiple quantum wells (MPQs) sandwiched between 36-pair *n*-type and 23-pair *p*-type $Al_{0.9}Ga_{0.1}$ As/$Al_{0.05}Ga_{0.95}$ As DBR layers with a single $Al_{0.98}Ga_{0.02}$ As layer (20 nm thickness) for oxidation. The photoluminescence (PL) measurement results show that the PL peak wavelength of our MQW active region is at around 924 nm at room temperature (RT). Based on the measured Bragg wavelength (∼937 nm) in our VCSEL cavity, the corresponding cavity-to-PL detuning wavelength is around 13 nm. Such a design can improve the high-temperature performance of the VCSEL [15]. The fabrication of the array starts with the Zn-diffusion process. A high-quality Si_3N_4 film is necessary to serve as the mask for the high-temperature diffusion process. The mask defined diameter of the optical aperture (without Zn-diffusion) is around 8 μm. By considering the lateral Zn-diffusion, the final W_z is around 7.5 μm after the finish of the Zn-diffusion process with a ∼1.7 μm depth (d). After the diffusion process, the mesa etching process is performed. An oxidation technique is then used to define a circular current-confined area 9.5 μm in diameter. The oxide layer for current confinement is removed from the oxide-relief structure by using selective wet chemical etching [10–15]. Due to the lower dielectric constant of air compared with that of the AlO_x layers, there is a demonstrated reduction in the parasitic capacitance and improvement in the VCSEL's speed for a single device or small scale array [10–15]. Here, in our large array, with its hundreds of VCSEL units, this would result in a large parasitic capacitance and a serious RC-limited bandwidth. It is expected that our oxide-relief technique can effectively release the burden imposed on the RC-limited bandwidth of the large VCSEL array for high-power performance. In addition, under high-power and high-current density operation, the reliability of the oxide-confined VCSEL is usually an issue. An improvement in the reliability of our oxide-relief structure can also be expected because of the elimination of oxide-layer-induced stress on the neighboring active layers [17]. After *p*-type contact metallization (Ti/Au; 50/200 nm), the device is passivated by a SiO_2 layer (∼150 nm) and an ∼3 μm thick polymethylglutarimide layer is then deposited for planarization. Finally, an ∼2 μm thick Ti/Au layer is evaporated onto the chip to arrange the different VCSEL units in a parallel array and for on-wafer probing. As shown in Fig. 1(a), the fabricated device has a 33 μm diameter active mesa and the *n*-type contact is realized in the bottom side of the *n*-type GaAs substrate to ensure uniform current distribution in the array structure.

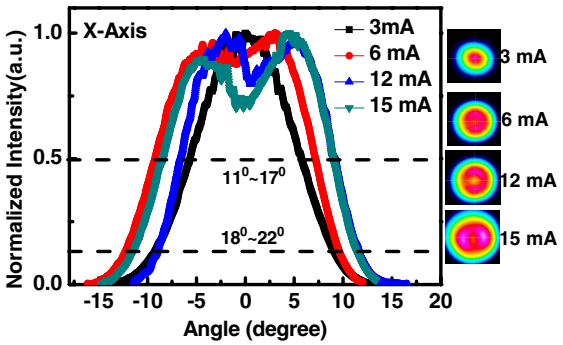

Fig. 3. One-dimensional (1D) (in the *x*-direction) and 2D far-field patterns of a single device measured under different bias currents ($W_o/W_Z/d$: 9.5/7.5/1.7 μm).

3. MEASUREMENT RESULTS

Figures 2(a) and 2(b) show the measured light output power (L), operating voltage (V), and optical spectra under different bias currents (I) and continuous-wave (CW) operation for a single VCSEL unit. As can be seen, the single device exhibits a threshold current of 0.7 mA and can sustain QSM operation (two modes) under the full range of bias currents (from threshold to saturation) with a maximum QSM power up to 7.1 mW. Figure 3 shows the measured one-dimensional (1D) (in the *x*-direction) and 2D far-field patterns of a single device under different bias currents. For 2D measurement, a charge-coupled device (CCD) camera is installed just above the array to take pictures of the far-field patterns. In order to avoid saturation of the camera and the influence of the optical feedback effect on the measured patterns, neutral density filters are inserted between the array and the CCD. The 1D patterns are constructed from the measured data points in our 2D patterns. We can clearly see that Gaussian-like FFPs can be sustained when the bias current is less than 3 mA. On the other hand, the FFP starts to become doughnut like with a shallow dip (<20%) in the center of the pattern when the bias current further goes higher. The observed shallow dip in our far-field patterns can be attributed to the characteristics of two competitive lasing modes (quasi-SM) in our VCSEL cavity, as shown in Fig. 2(b). The output optical spectra of our Zn-diffusion VCSEL are sensitive to the relative sizes of the Zn-diffusion and oxide-relief apertures [11].

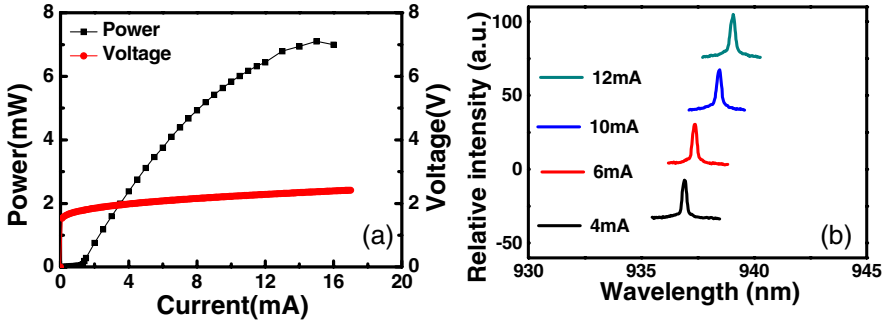

Fig. 4. (a) Measured L-I-V curve of a single-mode reference VCSEL unit, (b) measured optical spectra at different bias currents ($W_o/W_Z/d$: 10.5/7.5/1.7 μm).

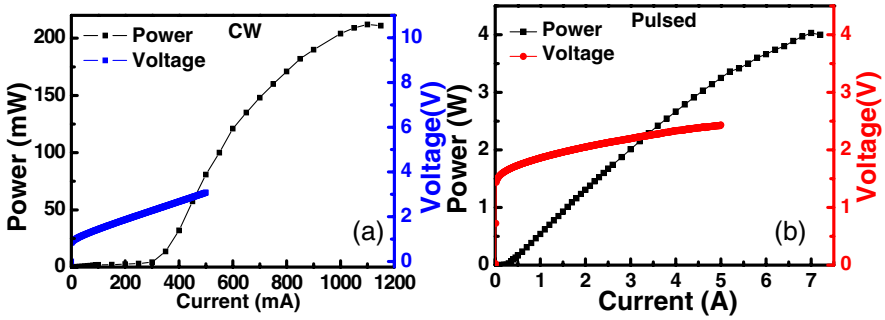

Fig. 5. L-I-V curves of our array measured under (a) CW and (b) pulsed mode operation, respectively.

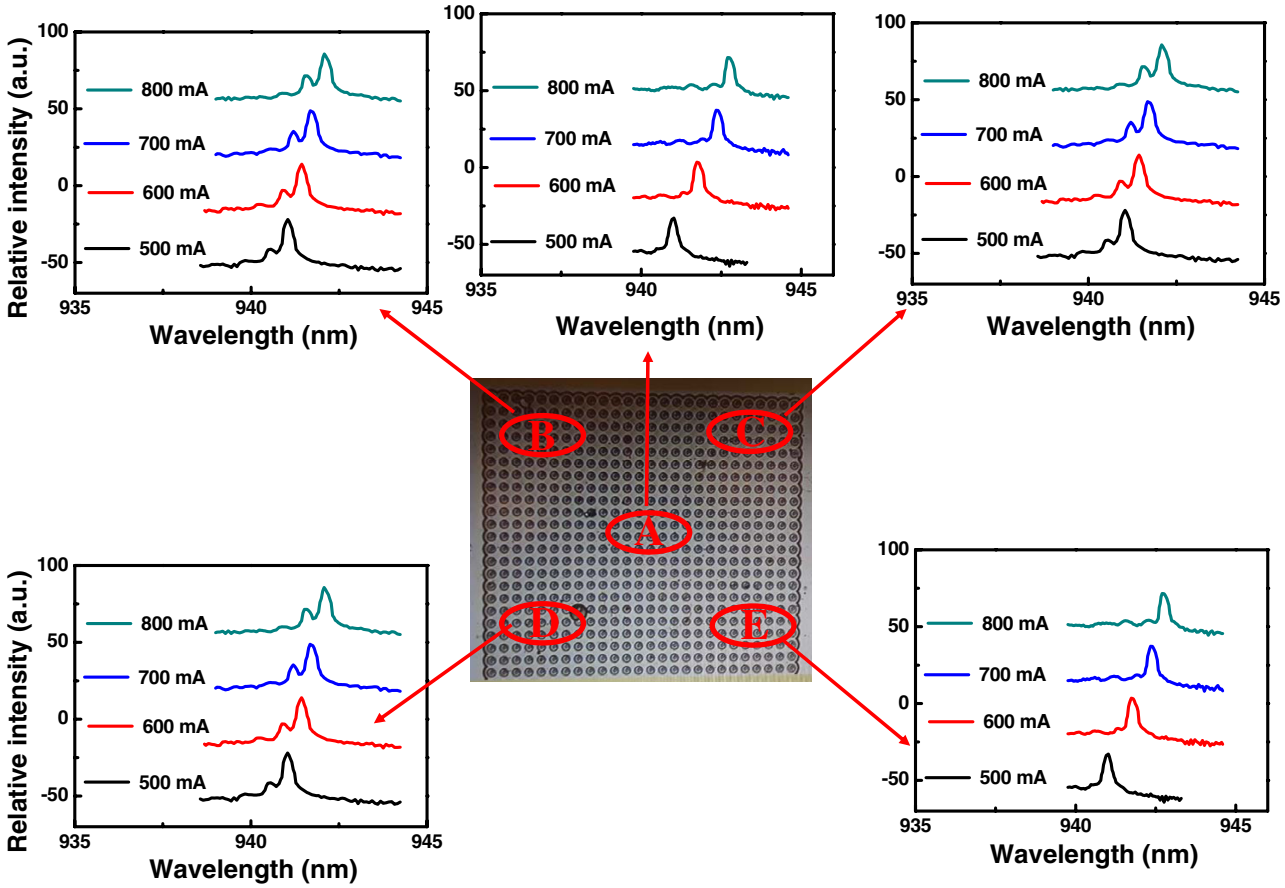

Fig. 6. Bias-dependent optical spectra measured at different positions on our array under continuous-wave (CW) operation.

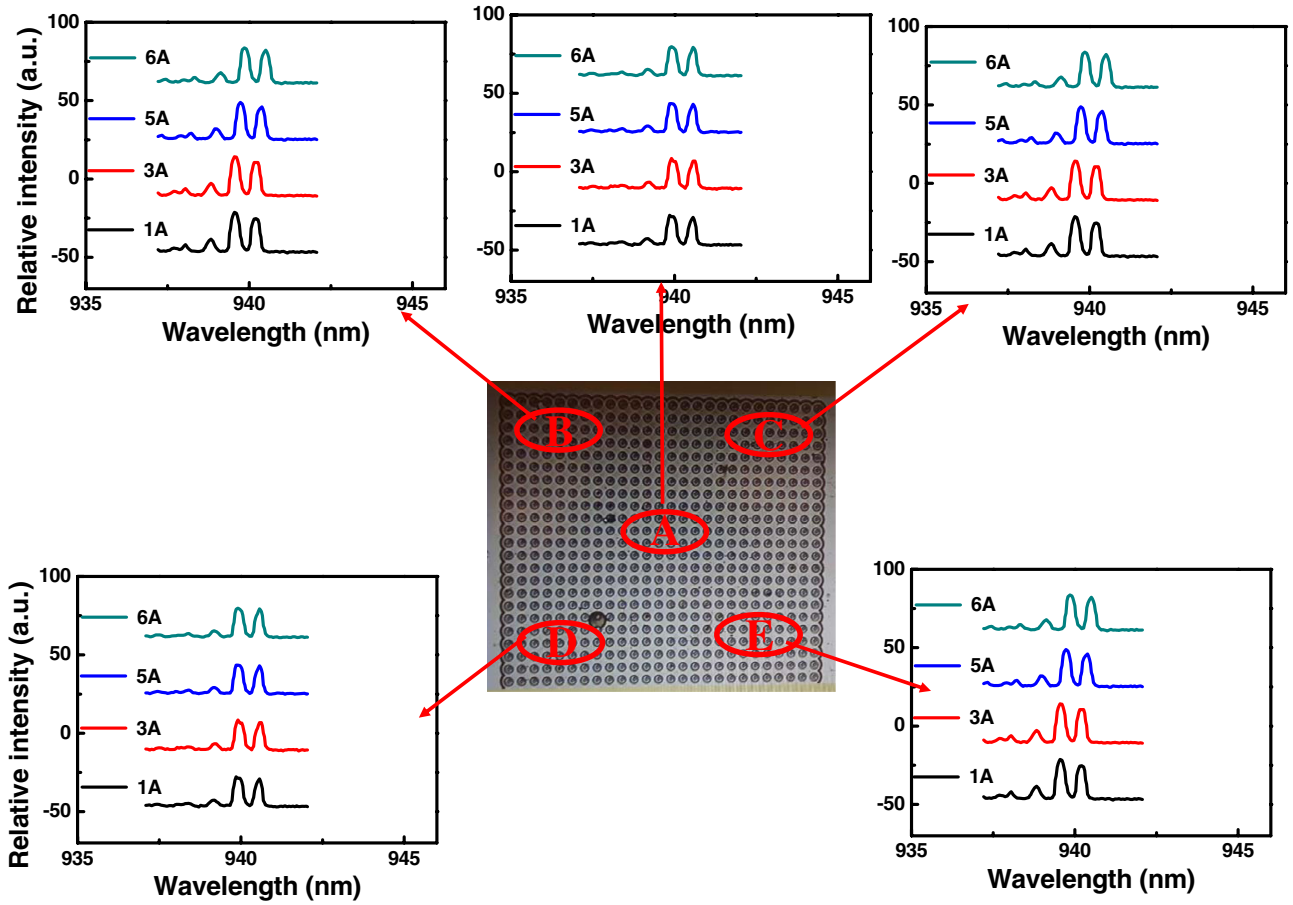

Fig. 7. Bias-dependent optical spectra at different positions on our array measured under pulsed mode operation.

Perfect SM operation can be realized by further increasing the sizes of the oxide-relief apertures to increase the intra-cavity loss in this Zn-diffused VCSEL [11]. Figures 4(a) and 4(b) show the measured L-I-V curves, and bias-dependent optical spectra obtained under CW operation for a single VCSEL unit with a larger oxide-relief aperture size (9.5–10.5 μm). As can be seen, perfect SM performance can be achieved under the full range of bias currents. However, the I_{th} is increased from 0.7 to 1.1 mA. This should result in a further increase of the operation current and junction temperature in our large array, which is the major bottleneck to its dynamic and static performance as will be discussed latter. We thus choose a single device structure ($W_o = 9.5$ μm) with QSM performance and moderate I_{th} value to assembly our array.

Figures 5(a) and 5(b) show the L-I-V curves for our array measured under CW and pulsed mode operation, respectively. Here, the current pulses, which are generated from the pulse current source (KEITHLEY 2461), have a 1 ms pulse width and a 1% duty cycle. We can clearly see that under pulsed mode operation our array can provide a maximum power of up to 4 W with a threshold current of around 0.4 A.

According to the single device L-I measurement results, shown in Fig. 3, these two numbers are reasonable for our array with up to 570 light emission apertures. In contrast to pulsed mode operation, the maximum output power is much lower under CW operation (~0.2 versus 4 W). This result indicates that a large bias current will induce significant device heating and degradation affecting the L-I performance of the array under CW operation.

Figures 6 and 7 show the bias-dependent optical spectra measured at different positions (A to E) on our array under CW and pulsed mode operation, respectively. During measurement, a multi-mode fiber with a ball lens tip is used to collect the light output from different locations on the array. We can clearly see that under both CW and pulsed mode operations the whole active area of our array exhibits stable (quasi-) SM performance from near threshold up to saturation output. In addition, in certain regions (A and E) of the chips, the measured optical spectra show a larger side-mode suppression ratio (SMSR) than that of traces measured at other positions (B to D). This phenomenon can be attributed to the fact that the output optical spectra of our VCSEL are sensitive to the relative size between the Zn-diffusion and oxide-relief apertures [11], as illustrated in Figs. 2 and 4.

The larger SMSR in regions A and E is thus due to the VCSEL units in these two regions having slightly larger sized oxide-relief apertures than that of devices in other regions (B to D). This leads to the induction of a larger intra-cavity loss by the Zn-diffusion area, which can more effectively suppress the transverse modes, thereby increasing the SMSR in the output optical spectra [11].

In contrast to CW operation, there is a negligible redshift in the central wavelength with an increase in the bias current under pulsed mode operation, which implies that the device-heating effect can be eliminated under 1% duty cycle pulsed mode operation. Furthermore, under CW operation, the magnitude of higher-order transverse modes in the measured optical spectra

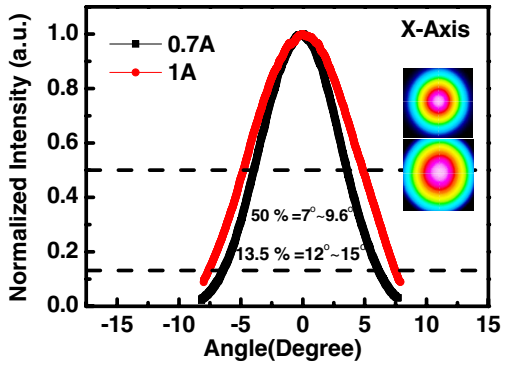

Fig. 8. Measured one-dimensional (1D) (in the x-direction) and 2D far-field patterns of the VCSEL array under lower pulse bias currents (0.7 and 1 A).

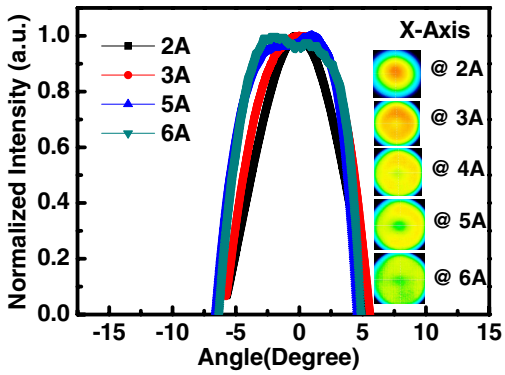

Fig. 9. Measured one-dimensional (1D) (in the x-direction) and 2D far-field patterns of the VCSEL array under higher pulse bias currents (2–6 A).

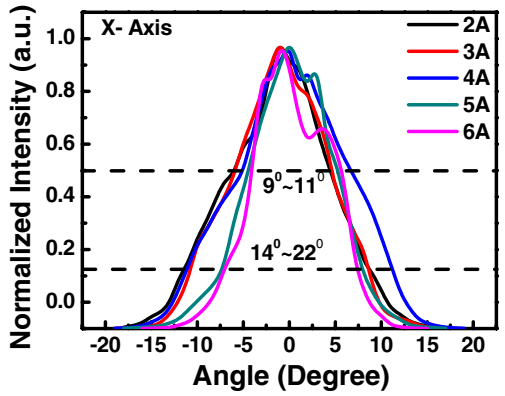

Fig. 10. 1D patterns measured using a rotating slit under pulsed mode operation.

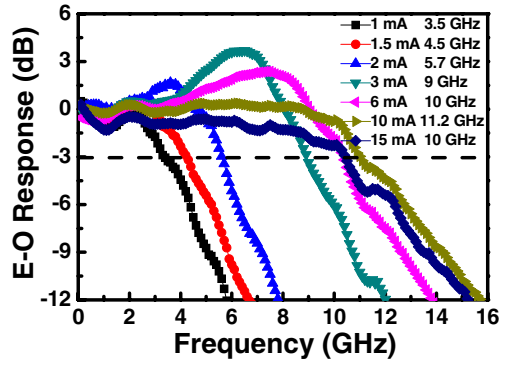

Fig. 11. Measured electrical-to-optical (E-O) frequency response of a single reference device at different bias currents.

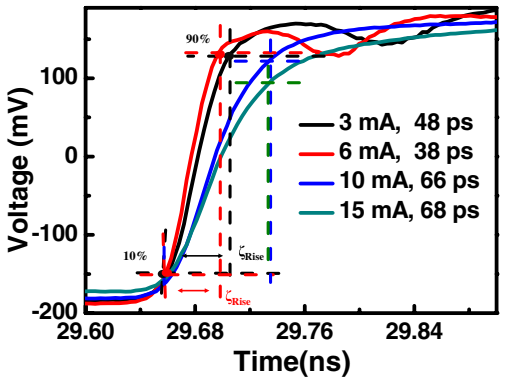

Fig. 12. Waveform of the rise time (t_r) of a single reference device measured at different operating currents.

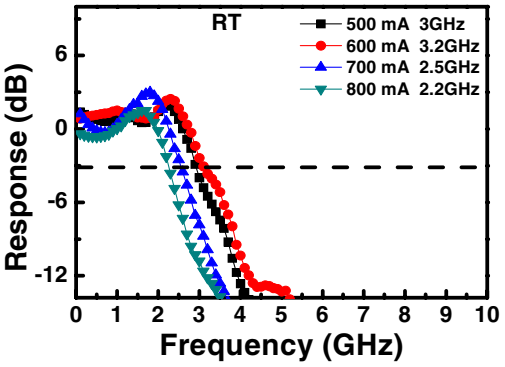

Fig. 13. Measured electrical-to-optical (E-O) frequency response of the demonstrated VCSEL array under CW operation.

becomes less than that which occurs under pulsed mode operation. The mechanism for this phenomenon can be understood as follows.

Higher-order transverse modes usually happen when the bias current increases. This is because the optical gain under a large bias current is high enough to support higher-order mode lasing. However, compared with pulsed mode operation, device heating is much more serious under CW operation, with higher junction temperatures and a more significant redshift in the central wavelengths with the increase of the bias current, as discussed above. This kills the optical gain due to the thermal-induced carrier leakage from the MQWs and impedes lasing in the higher-order modes, where a higher threshold gain is needed than in the fundamental mode [13].

Figure 8 shows the 1D (in the x-direction) and 2D far-field patterns of the VCSEL array measured under lower bias currents (0.7 and 1 A) and pulsed mode operation. As can be seen, a perfect Gaussian mode can be attained when the average bias current to each VCSEL unit is less than 2 mA and SM performance can thus be expected, as illustrated in Figs. 2 and 3. When there is a further

increase in the pulsed bias current, the CCD is usually saturated by the peak optical power. In order to reduce the illuminated power density onto the CCD, we must increase the distance between the CCD camera and the array.

However, due to diffraction of the optical beam, the optical spot becomes larger than the aperture size (1 cm × 1 cm) of the CCD so it cannot be captured in its entirety. A different approach was adopted for 1D FFP measurement to get accurate divergence angles under peak power. A rotational arm connected to a well-calibrated optical sensor head with a slit mounted on its window is used. The distance between the sensor head and the device being tested is around 13 cm. During measurement, the width of the slit is set to be less than 1 mm. With a distance of 13 cm between the slit and the device being tested, the resolution for divergence angle measurement should be around 0.44 deg. Such a resolution is high enough to accurately measure the divergence angles with the values presented in this paper. Figure 9 shows the 1D and 2D patterns measured by the CCD camera. Although such an approach cannot capture the whole optical spot, as noted above, we can still investigate the optical mode field distribution around its peak. As can be seen, a shallow depression appears in the peak of the far-field pattern when the pulsed current is over 3 A, which corresponds to an average bias current of around 5 mA on each light emission aperture.

The results are consistent with the measurements for the single device, which shows a doughnut-like pattern when the bias current is over 3 mA, as illustrated in Fig. 3. Figure 10 shows the FFP measured using a rotating slit. A narrow $1/e^2$ far-field pattern (<20°) can still be sustained under a bias current of near around maximum output power.

Figures 11 and 12 show the measured E-O frequency response and waveform of the rise time (t_r) for a single reference device. As can be seen, the E-O bandwidth (10 GHz) measured under a 6 mA bias current is consistent with the measured rise time ($0.35/t_r$). In addition, there is an observable degradation in the E-O bandwidth when the dc bias current reaches 15 mA. This occurs under such a high dc bias current, because of the saturation of the CW output optical power, which represents the decrease in differential gain and the modulation speed of the device. By further increasing the indium mole fraction (compressive strain) inside our active layers, such degradation in speed can be minimized due to the increase of conduction band offset [13].

Figure 13 shows the measured E-O frequency response of the demonstrated VCSEL array under CW operation. As can be seen, the highest E-O bandwidth (3.2 GHz) measurement happens under a 600 mA CW bias current. A further increase in the bias current leads to degradation in the E-O bandwidth due to the thermal effect. Compared with the E-O bandwidth of a single reference device measured under the same averaged bias current (~1 mA), as shown in Fig. 10, our array exhibits a similar E-O bandwidth value (3.2 versus 3.5 GHz).

This result implies that our oxide-relief technique can effectively minimize the parasitic RC-limited bandwidth in a large area array and that its dominant E-O bandwidth limiting factor under CW operation is the thermal effect.

The equivalent circuit modeling technique is adopted to investigate the external RC-limited bandwidth of the array and the single reference device [12,13]. A schematic diagram of the equivalent circuit model is shown in Fig. 1(c) and the physical meaning of each circuit element is specified in Table 1. Figure 14(a) shows

Table 1. Values of the Circuit Elements Used for the Fitting Processes

	Physical Meaning	1 mA, Single Device	600 mA, Array
R_{pad} (total)	Pad resistance (Ω)	10	0.118
L_{pad} (total)	Pad inductance (nH)	0.035	8
C_p (total)	Parasitic capacitance (pF)	0.235	145.8
R_c (total)	Contact resistance (Ω)	85	0.21
C_0	Oxide layer capacitance (pF)	0.250	152.3
R_a	Diffusion resistance (Ω)	65	0.112

the measured and fitted S_{11} traces (microwave reflection coefficients) on a Smith chart for a single device and the array under bias currents of 1 and 600 mA, which corresponds to the same average bias current (~1 mA) on each single VCSEL unit. As can be seen, the measured and simulated traces match very well from near 1 to 15 GHz. Table 1 gives the extracted circuit element values for both devices. Much larger values of parasitic capacitance (C_p) and oxide layer capacitance (C_o) are observed in our array than for the single reference device because there are nearly 600 single VCSEL units in parallel inside. The extracted C_o value of single (array) device is quite close to its theoretical value of 0.275 (165) pF. The theoretical value of C_o can be obtained according to the single oxide layer thickness (25 nm), diameters of the oxide-aperture (active mesa) 10 (33) μm, and the dielectric constant (1) of free-space. In addition, the much larger area of the metallic electrodes in our array than in the single device (1.7×1.7 mm^{2}versus ~ 100 μm^2), as shown in Fig. 1(b), results in a dramatic increase of parasitic inductance (L_{pad}). Such a large L_{pad} results in a "knot" (L-C resonance) in its S_{11} trace on the Smith chart and greatly releases the RC-limited bandwidth of our VCSEL array. If the L_{pad} in our equivalent circuit model is removed, the simulated RC-limited 3 dB bandwidth of our array would be far less than 1 GHz. Figure 14(b) shows the extracted RC-limited frequency responses of the two devices under the same average bias current (~1 mA). Thanks to the oxide-relief process and inductance-induced resonant effect, which effectively enhances the RC-limited bandwidth, our array exhibits a 4.7 GHz RC-limited bandwidth, which corresponds to a rise time of around 75 ps (t_r). Figure 15 shows the waveform of the rise time (t_r) of our array measured under different CW pre-bias currents. We can clearly see that under the optimum pre-bias current of 0.6 A for the highest E-O bandwidth, the measured t_r can be as short as 98 ps. Compared to the commercially available 940 nm VCSEL array with a close value of output power (~2.5 W) under the same bias current, around 3.5 A, our device exhibits a much faster rise/fall time (98 ps versus 1 ns) [16] under a lower pre-bias current (0.6 versus 3 A).

A faster speed performance can be expected for our array operated under pulsed mode operation to minimize the thermal effect. However, the pulsed current source used to drive our device has a much longer t_r (several nanoseconds) than the intrinsic response time (<100 ps) of the array itself. A faster pulse current source, which can deliver a peak output current of tens of amperes and has

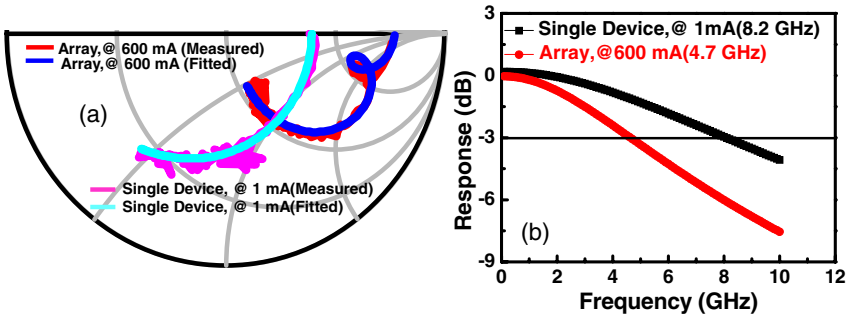

Fig. 14. (a) Measured and fitted S_{11} traces (microwave reflection coefficients) on a Smith chart for single device and the array under bias currents of 1 and 600 mA. (b) RC-limited frequency responses for the two devices extracted under the same average bias current (∼1 mA).

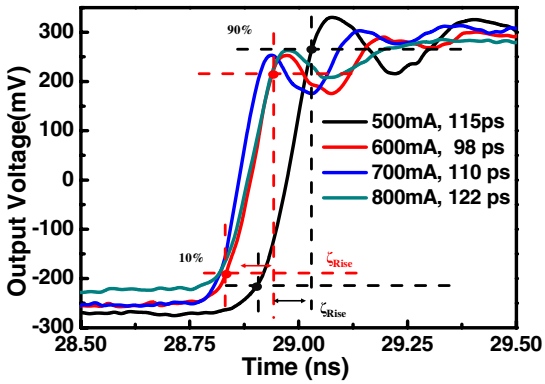

Fig. 15. Rise time (t_r) waveforms of our array measured under different CW pre-bias currents.

a response time as short as sub-nanoseconds, is highly desired for our applications [18].

4. SUMMARY

With the help of oxide-relief and Zn-diffusion techniques we fabricate and demonstrate a high-power VCSEL array with a fast response time. The highly uniform Zn-diffusion apertures can effectively suppress the lasing of higher-order transverse modes across the whole array. A stable quasi-SM output from near the threshold current up to the saturation output with a maximum output power of 4 W (1% duty cycle) and unchanged single-spot far-field patterns with narrow divergence angles ($1/e^2$: around 14°) under 4 W output have been successfully demonstrated. Furthermore, the parasitic RC-limited bandwidth in our array can be greatly released due to the oxide-relief process and parasitic inductance-induced resonant effect. Under the same averaged CW bias current (∼1 mA) as that of a single reference VCSEL, our array can exhibit a similar net 3 dB E-O bandwidth (∼3.5 GHz) value. This result indicates that it is the thermal effect rather than the RC-limited bandwidth which is the major factor limiting the speed of our array with oxide-relief apertures under CW operation. Under the optimum CW pre-bias current, our array can exhibit a fast rise time as short as 98 ps under pulsed voltage driving.

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