Flip-Chip Bonding Packaged THz Photodiode With Broadband High-Power Performance

Jhih-Min Wun, Cheng-Hung Lai, Nan-Wei Chen, John E. Bowers, and Jin-Wei Shi

***Abstract*— Design and analysis of the flip-chip bonding package for near-ballistic unitraveling-carrier photodiodes (NBUTC-PDs) with reliable high-power performance from dc to sub-THz (∼300 GHz) frequency has been demonstrated. According to our simulation and measurement results, the geometric size of flip-chip bonding structure becomes a major limitation in speed and output power when the operating frequency is over ∼100 GHz. In order to overcome this problem, the position of Au/Sn bump on bottom AlN substrate for bonding process, must be as close as possible with the active PD mesa on the InP substrate at topside. Compared with the control with a longer spacing (∼90 versus 25 μm), our device not only exhibits a broader bandwidth (225 versus 200 GHz), but also a higher saturation current (13 versus 9 mA). With such an optimized flip-chip bonding structure for package of NBUTC-PD, a wide 3-dB bandwidth (∼225 GHz), high saturation current (13 mA), and a 0.67-mW maximum output power at 260-GHz operating frequency have been achieved simultaneously.**

***Index Terms*— Photodiodes, packaging.**

I. Introduction

ULTRA-FAST photodiodes (PDs) serve as the key component, which usually determines the maximum allowable operating frequency and dynamic range, in the MMW (THz)-over-fiber systems, such as, photonic sub-THz wireless communication system [1], [2] and photonic MMW measurement instrument [3]. Uni-traveling carrier photodiodes (UTC-PDs) [3], [4], which have only fast electron as active carriers, have demonstrated record optical-to-electrical (O-E) bandwidth (310 GHz) at 1.55 μm optical wavelength by use of on-wafer measurement setups [4]. However, its practical application is restricted by its small output power, which is mainly due to the low load resistance (12.5 Ω), and low responsivity (<0.01 A/W). To develop a package structure for sub-THz PD with wide-bandwidth, high output power, and reasonable responsivity performances is thus very important. Recently, high output power (∼1 mW) has been demonstrated at 300 GHz by use of a well-packaged photomixer module, which is composed of a pair of UTC-PDs embedded in WR-3 waveguide with power combing structure on quartz substrate [5]. Such power level and bandwidth are comparable with those of high-performance and commercial available MMW frequency amplifier/multiplier chain.[1] Nevertheless, its frequency response can't cover from dc due to the characteristics of waveguide based approach and resonant type of impedance-matching circuit (short-stub) [5]. A PD module, which is composed of a ultrafast PD chip and a broadband bias tee network,[2] with staring frequency from dc and up to hundreds of GHz is highly desired for the application of photonic MMW measurement instrument, such as network analyzer (NA), which eliminates the necessity of different metallic waveguide based NA extenders (for measurements at different MMW bands) over such wide frequency regime [3].

The flip-chip bonding package of PD onto co-planar waveguide (CPW), which is fabricated on ceramic substrate such as, aluminum nitride (AlN), is one possible solution to have hybrid integration with ultra-broadband bias tee network, mitigate the device heating problem of PD, benefit the optical coupling, and achieve hundreds of 3-dB bandwidth (from dc) of whole packaged module [6]–[8]. In our previous work, by greatly downscaling the area of bonding bumps (∼15 × 20 μm^2) of a miniaturized size NBUTC-PD, we have demonstrated excellent performance in terms of bandwidth and output power (−1.8 dBm) at around 300 GHz frequency [8]. However, the mechanical strength between bonded device and CPW lines is too weak to have high reliable operation. In this letter, a novel design of CPW pads at nearly 300 GHz sub-THz frequency regime for robust and high-yield flip-chip bonding package has been proposed. A significant enhancement (∼3 dB) in speed and output power over a wide range of measured frequency (∼75 to 300 GHz) can be achieved by shortening the current transition region (from active PD chip to the Au/Sn bump on AlN substrate) in our package. Based on this, excellent performances of speed (225 GHz 3-dB bandwidth), saturation current (13 mA), and output power (0.67 mW) at 260 GHz of the flip-chip packaged NBUTC-PD chips have been successfully demonstrated.

II. Device Structure and Design

The detail epi layer structures and fabrication processes of studied NBUTC-PD chip can be referred to our previous works [6]. It has a 3 μm active diameter and a 190 nm collector layer thickness under −2 V bias. Figure 1(a) shows the top-view of the active PD chip, CPW lines (with Au(0.8)/Sn(0.2) bumps on it) on the AlN substrate, and PD chips after flip-chip bonding. To downscale the geometric size of CPW lines, which include the widths of center strips and air gap, is the most

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[1]Virginia Diodes, Inc., 979 Second Street, S.E. Suite 309, Charlottesville, VA 22902-6172. Model of Product: WR3.4 AMC.

[2]Finisar Corporation, 1389 Moffett Park Drive, Sunnyvale, CA 94089-1133, Model of Product: XPDV412xR.

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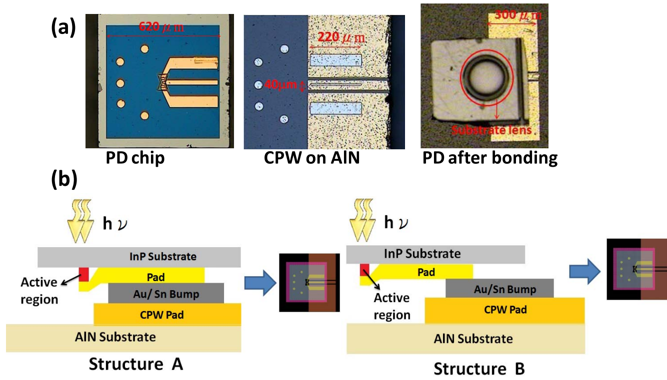


Fig. 1. (a) Top-view (before and after flip-chip bonding) and (b) cross-sectional view (after flip-chip bonding) of structures A and B. The insets in (b) show the top-view layouts of both structures after flip-chip bonding.

effective way to suppress the radiation loss at sub-THz regime and enhance the bandwidth of CPW lines for package [9]. However, this would reduce the area of Au/Sn bumps for bonding and result in a poor adhesion between active PD chip and AlN substrate. In order to overcome such problem, a long and narrow micro bumps are implemented on the center strip and ground planes of CPW lines. The detail geometric sizes of CPW lines on the InP based NBUTC-PD chip and AlN substrate (with bumps) are specified on Figure 1(a). Figure 1(b) shows the conceptual cross-sectional view of two different kinds (A and B) of bonded chips and their corresponding layouts. Here, two flip-chip bonding structures (A and B) were fabricated and characterized. These two structures share the same geometric structures of passive CPW lines on AlN substrate and the same active NBUTC-PD chip. The main difference between structures A and B is their different lengths of current transition region (∼25 vs. ∼90 μm), which means the distance of current flow path from active PD chips on the top-side through the passive Au/Sn bump and to the CPW lines on the bottom side. Based on the point of good heat-sinking of PD, the position of Au/Sn bump should be just buried below the active PD mesa [10], which can directly sink the generated heat from device to AlN substrate with a shortest length of path. However, for the PD with such a miniaturized size (3 μm diameter), this flip-chip bonding structure would easily damage the PD and result in a low yield of bonding process. Furthermore, when the operating frequency reaches sub-THz regime, different lengths of current transition region may have serious influence on the dynamic performance of flip-chip bonding devices.

Figure 2(a) and (b) shows the device structures used for the high-frequency simulation[3] and the simulated MMW frequency response of transmission coefficient (S_{12}) of structures A to C, respectively. Here, in our simulation the active PD has been assumed as an ideal current source with infinite large 3-dB bandwidth. We can clearly see that structure A shows a wider bandwidth and less high-frequency roll-off than that of structure B and C, which has a further increased current transition path (D) to 150 μm. The superior MMW performance of structure A with the shortening of D can be attributed to the minimization of MMW reflections induced bandwidth degradation between active PD and passive Au/Sn bumps on the CPW lines.

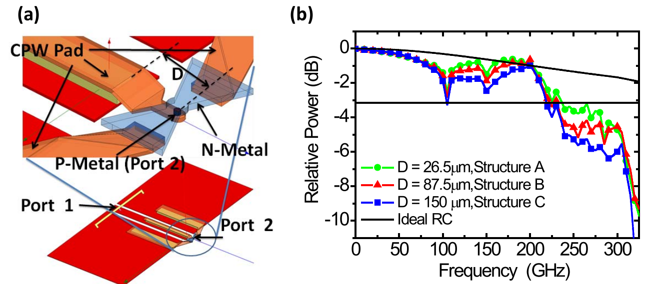


Fig. 2. (a) The geometric structure used for high-frequency simulation. For clearance, the color of AlN and InP substrates are both set as transparent. (b) The simulated S_{12} frequency responses of structure A, B, and C. The extracted ideal RC-limited frequency response of PD is shown as solid line.

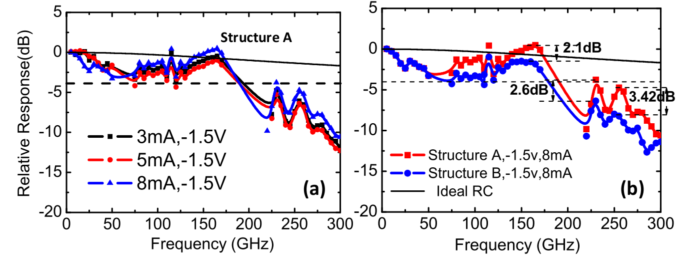


Fig. 3. (a) Photocurrent dependent O-E frequency responses measured under a fixed reverse bias of structure A. (b) Measured O-E frequency responses of structures A and B. The extracted ideal RC-limited frequency response of PD is shown as solid line.

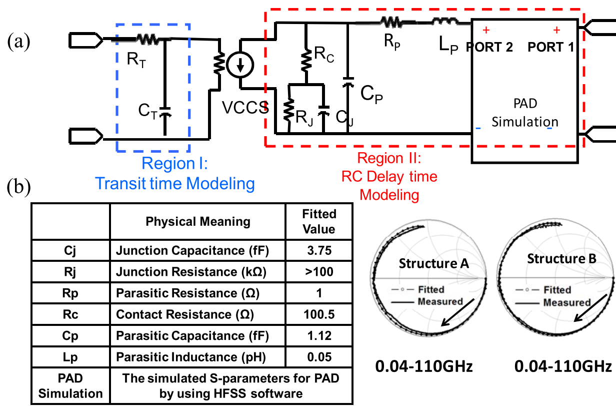
III. Measurement Results and Discussion

The measured dc responsivity of our device with a 3 μm active diameter is around 0.08 A/W. The dynamic performance is measured with a heterodyne beating system. A power meter with two different sensor heads (dc to 50 and 75-110 GHz) is used for the range from dc to 110 GHz. When the measurement frequency is greater than 110 GHz, a thermal MMW power meter (PM4, VDI-Erickson) is used. The maximum measurement bandwidth for our system is limited by our WR-3.4 waveguide based MMW probe at 325 GHz. During our measurement, the insertion losses of waveguide probe (4 ∼ 5 dB for WR-3.4 (220-325 GHz) waveguide probe), WR-10 waveguide section (0.3 dB at 260 GHz), and waveguide taper (0.5 dB at 260 GHz),[4] have been carefully de-embedded. Figure 3(a) shows the measured optical-to-electrical (O-E) frequency responses of structure A from near dc to 300 GHz under a fixed reverse bias (−1.5 V) and different output photocurrents (3, 5, and 8 mA). Figure 3(b) shows the measured O-E frequency responses of structure A and B under the same reverse bias (−1.5 V) and output photocurrent (8 mA). Each trace is normalized to the same reference value for fair comparison. As can be seen, the maximum 3-dB bandwidth of A is around 225 GHz and its output power is around 2 ∼ 3 dB higher than that of B when the operating frequency is over 75 GHz. The trends of these measurement results are consistent with our simulation, as discussed in Figure 2.

In order to investigate the bandwidth limiting factors of whole flip-chip bonding module, we adopt two-port equivalent-circuit-models, which include the two bandwidth-limiting factors (i.e., carrier transit time (f_t) and RC delay

[3]ANSYS, Inc., Southpointe, 275 Technology Drive, Canonsburg, PA 15317, USA. Model of Product: HFS.

[4]Virginia Diodes, Inc., 979 Second Street, S.E. Suite 309, Charlottesville, VA 22902-6172. VDI APPLICATION NOTE: Power Measurement above 110 GHz.



	Physical Meaning	Fitted Value
Cj	Junction Capacitance (fF)	3.75
Rj	Junction Resistance (kΩ)	>100
Rp	Parasitic Resistance (Ω)	1
Rc	Contact Resistance (Ω)	100.5
Cp	Parasitic Capacitance (fF)	1.12
Lp	Parasitic Inductance (pH)	0.05
PAD Simulation	The simulated S-parameters for PAD by using HFSS software	

Fig. 4. (a) Equivalent-circuit-model used. (b) Measured (continuous line) and fitted (open circles) S_{11} parameters from near DC to 110 GHz under a fixed dc bias (−2 V). The arrow heads indicate the increase in the sweeping frequency. The inserted Table shows the values of circuit elements used in fitting process.

time (f_{RC}),) [6], as shown in Figure 4(a). In this model, the "pad simulation block" is just the simulation result what we have discussed in Figure 2. The fitted values of each circuit element, except for R_T and C_T, is shown in the Table inserted into Figure 4(b). During our device modeling process for the extraction of extrinsic f_{RC} of PD chips, such two artificial circuit elements have been removed due to that they are used to mimic the low-pass frequency response of internal carrier transient time [6]. Figure 4(b) shows the measured and simulated frequency responses for the S_{11} reflection coefficient parameter under a −2V bias of structure A and B; see the Smith chart. Clearly, the simulated and measured results of both structures match very well, from 10 MHz to 110 GHz. In addition, the length of structure B's trace (on Smith chart) is longer than that of structure A, which represents that the MMW signal in structure B would suffer from the larger phase-shift and more serious high-frequency roll-off, as discussed in Figure 2. By excluding the "PAD simulation block" in our equivalent circuit model, we can get the intrinsic RC-limited frequency response of our active PD. Such frequency response is shown as solid traces in Figure 2 and 3. We can clearly see that the RC-limited 3-dB bandwidth (up to 600 GHz) is much larger than that of flip-chip bonding package induced bandwidth limitation (∼250 GHz). This result implies that by optimizing our package structure to effectively drain the output power from PD, THz operation is possible.

Figure 5 shows the measured photo-generated MMW power at 260 GHz versus output photocurrent under a fixed reverse bias (−2 V) of structures A and B. The ideal relation between the MMW power and averaged photocurrent (solid line) with a 100% optical modulation depth under a 50 Ω load is also plotted for reference. Here, two chips for each bonding structure (A-1/A-2 and B-1/B-2) are shown in this Figure for references. As can be seen, structure A not only shows a 2 ∼ 3 dB higher output power under the same operation photocurrent but also exhibits a larger saturation current (13 vs. 9 mA) than structure B does. The superior saturation power performance of structure A to that of B (4.8 dB improvement) can be attributed to that in structure A the An/Sn bump is closer to the active PD (∼27 vs. ∼88 μm), which would benefit heat-sinking of device under high-power operation [10], as discussed in Figure 1. The maximum output

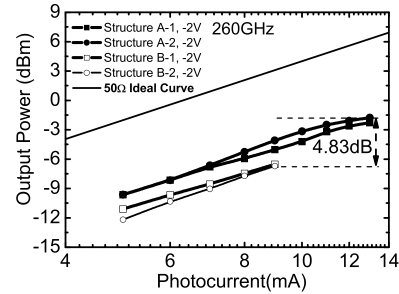


Fig. 5. The measured photo-generated MMW power versus photocurrent from structure A (A-1, A-2) and B (B-1, B-2).

power at 260 GHz operating frequency of structure A is as high as −1.77 dBm (∼0.67 mW), which is usually limited by thermal failure. Regarding with the field collapse effect inside collector layer of device A, it is not the major limiting factor for the achieved saturation current (13 mA) here according to our electric-field simulation result.

IV. Conclusion

Flip-chip bonding packaged NBUTC-PD for high-power and wideband (dc to 300 GHz) performance has been demonstrated. By greatly shortening the distance between bump and active PD mesa to ∼20 μm, a significant improvement in both speed and saturation current have been observed. These results suggest that for sub-THz operation, a careful design of PD flip-chip bonding structure is necessary to balance the trade-offs among speed, heat-sinking, and yield of package.

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