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| **Question** | **Q3** |  | **Name** |  |
| **Your score** |  |  | **Student ID** |  |
| **Full score** | **20** |  |  |  |

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| EE3046 Microcomputers Theory and Laboratory, 2022 Spring Semester  **Final Exam (8051)** *Scope*: CPU design*Time*: 18:00~20:50 |

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| |  |  | | --- | --- | | Best viewing mode for this question sheet in Microsoft Word program |  |      |  |  | | --- | --- | | File download | 9876543210陳小美Q3.circ **(Note: This is the solution to Q2)**  myLib  TP02.am  2021Fall-FinalExam - Q3.docx | | Answer upload | Enter your answers online. | |

Section 2：

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| Q3. (20%) Microinstruction design for 『JZR Rn,offset』 |

The file 『EE3046Sprin2022FinalExam - Q2 solution.circ』 is the solution to Q2 of Section 1.

Please design the microinstruction for 『JZR Rn,offset』 to be run in this circuit。.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Bit no. (Hex) | 1F | 1E | 1D | 1C | 1B | 1A | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 0F | 0E | 0D | 0C | | 0B | 0A | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |  |  |  |  |  |  |
|  |  |  | Sel\_ opcode or operand | | Flag value for disabling offset | sel PC in (= instru. Length) | | | Sel of flag | | | En of μPC counting | Sel\_ RAM addr | | Sel\_ RAM Din | |  | En\_ RAM Addr Lat | En\_ RAM Dout Lat | Str RAM | |  |  | Sel\_ ALU Bin | | Sel\_ ALU | | | |  |  | En of Cy update | En\_ Acc update | μP code in hexa-decimal | Assembly | Machine code | Length | Cycles  (Ours) | Cycles  (Official) |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 60 | - | - | ？ | ？ | ？ | ？ | ？ | ？ | ？ | ？ | ？ | ？ | ？ | ？ | ？ | ？ | - | ？ | ？ | ？ | | - | - | ？ | ？ | ？ | ？ | ？ | ？ | - | - | ？ | ？ | ???????? | JZR Rn,offset | 11001nnn offset | 2 | 1 | N.A. |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Please enter your answer to the following places. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 60 |  |  | W01 | | W02 | W03 | | | W04 | | | W05 | W06 | | W07 | |  | W08 | W09 | | W10 |  |  | W11 | | W12 | | | |  |  | W13 | W14 |  |  |  |  |  |  |

**Test program:**

You can verify the functionality of the microinstruction that you have designed by running the test program TP02.asm (shown below).

The ROMs in this circuit 『9876543210陳小美Q3.circ』 are filled with necessary data except the microinstruction of 『JZR Rn,offset』. So, you have to fill in it to μPM.

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| Content of TP02.asm   |  | | --- | | ; This is TP02.asm for Q2 of EE3046Spring2022 final exam.  ; In this program, DJNZ should be changed to JZR to be run in our 8051 CPU circuit.  ; Purpose of TP02.asm = to check the functionality of the microinstruction of new instruction JZR.  ; How to check: If JZR microinstruction works correctly, this program will end at LB10.  ; Otherwise, it may end at LB09 or stall at somewhere else.    0000| NOP  LB01:  0001| MOV R3, #LB02  0003| MOV A,#0H  0005| DJNZ R3,6H ; Should jump to LB03  0007| JMP LB09  ORG 20H  LB02:  0020| NOP  0021| NOP  0022| NOP  0023| NOP  0024| JMP LB09  LB03:  0026| MOV R3,#LB05  0028| MOV A,#0H  002A| DJNZ R3,0F2H ; Should jump to LB04  002C| SJMP LB09    ORG 40H  0040| JMP LB09  LB04:  0042| MOV R3,#LB09  0044| MOV A,#55H  0046| DJNZ R3,2H ; Should not jump.  0048| JMP LB10  ORG 50H  LB05:  0050| JMP LB09    ; The execution may end up jumping to LB09 if any branch is incorrect.  LB09:  0052| MOV R7,#0FFH  0054| JMP LB09  ; The execution will eventually reach LB10 if all branches are correct.  ORG 60H  LB10:  0060| MOV R7,#77H  0062| JMP LB10 | | **How to verify the correctness of JZR：**  If your microinstruction is **incorrect**, the program execution will end at **LB09** or stall at somewhere else.  If your microinstruction is **correct**, the program execution will end at **LB10**.  **Note:** In the file TP02.asm, you have to change all the “DJNZ”s into “JZR”s. |